AKTU

B.Tech III-Sem

Digital System Design

Unit-5 Lecture-1

EC & EC Allied



GATEWAY CLASSES

Gateway classes

UNIT 5 : Digital-to-Analog converters (DAC)

Lec 1

Today's Target

- Digital to Analog Converter
- Weighted Resistor DAC
- R-2R Ladder DAC
- University Questions

Gateway classes

UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
22-23 20-21 19-20	With neat diagram explain the operation of R-2R DAC	10 Marks
22-23	Explain a Weighted Resistor digital to analog convertor	10 Marks
19-20	The basic step of a 9-bit DAC is 10.3V. if 000000000 represents O Volts, what is the output for an input of 101101111 ?	2 Marks

Gateway classes

Digital to Analog Converter

- A Digital to Analog Converter (DAC) converts a digital input signal into an analog output signal.
- The digital signal is represented with a binary code, which is a combination of bits 0 and 1.
- A Digital to Analog Converter (DAC) consists of a number of binary inputs and a single output.
- In general, the number of binary inputs of a DAC will be a power of two.



Gateway classes

Types of DACs

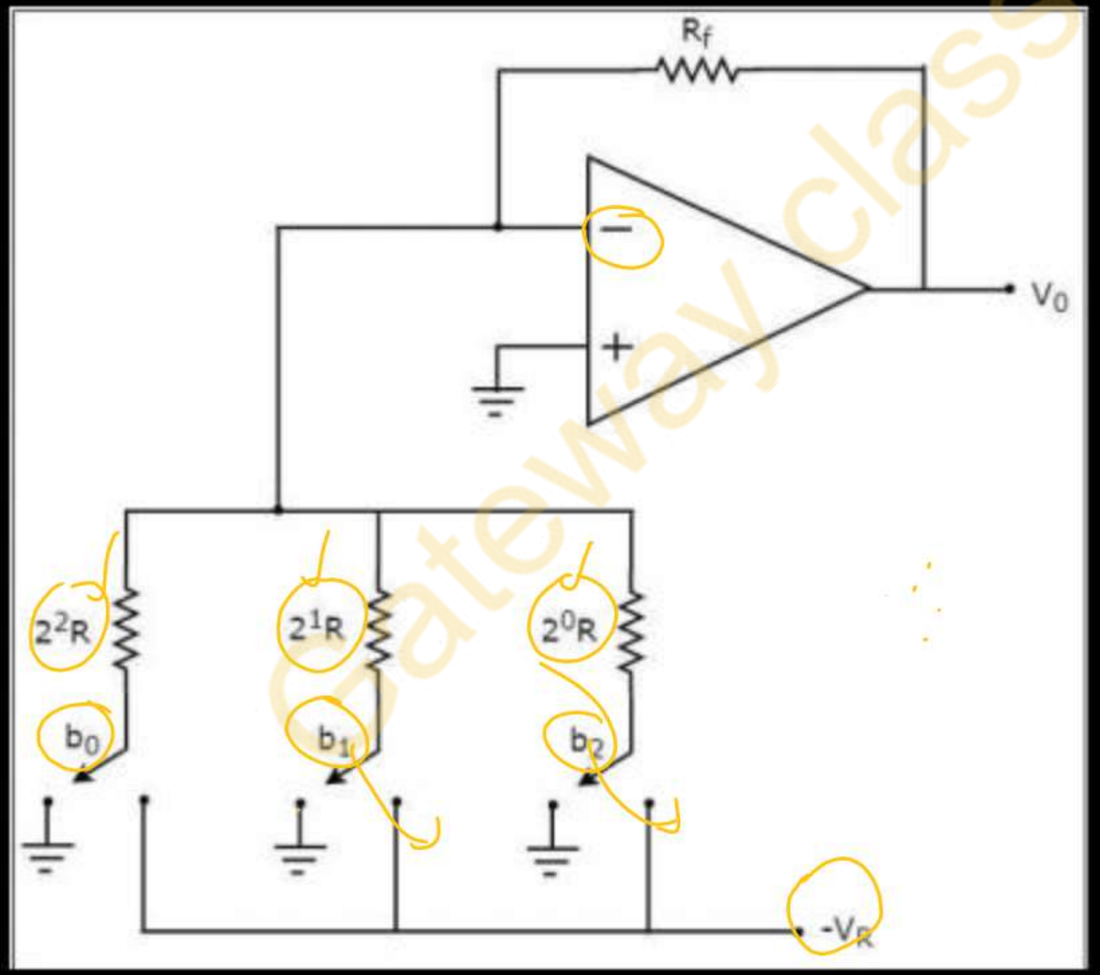
There are two types of DACs

- Weighted Resistor DAC
- R-2R Ladder DAC

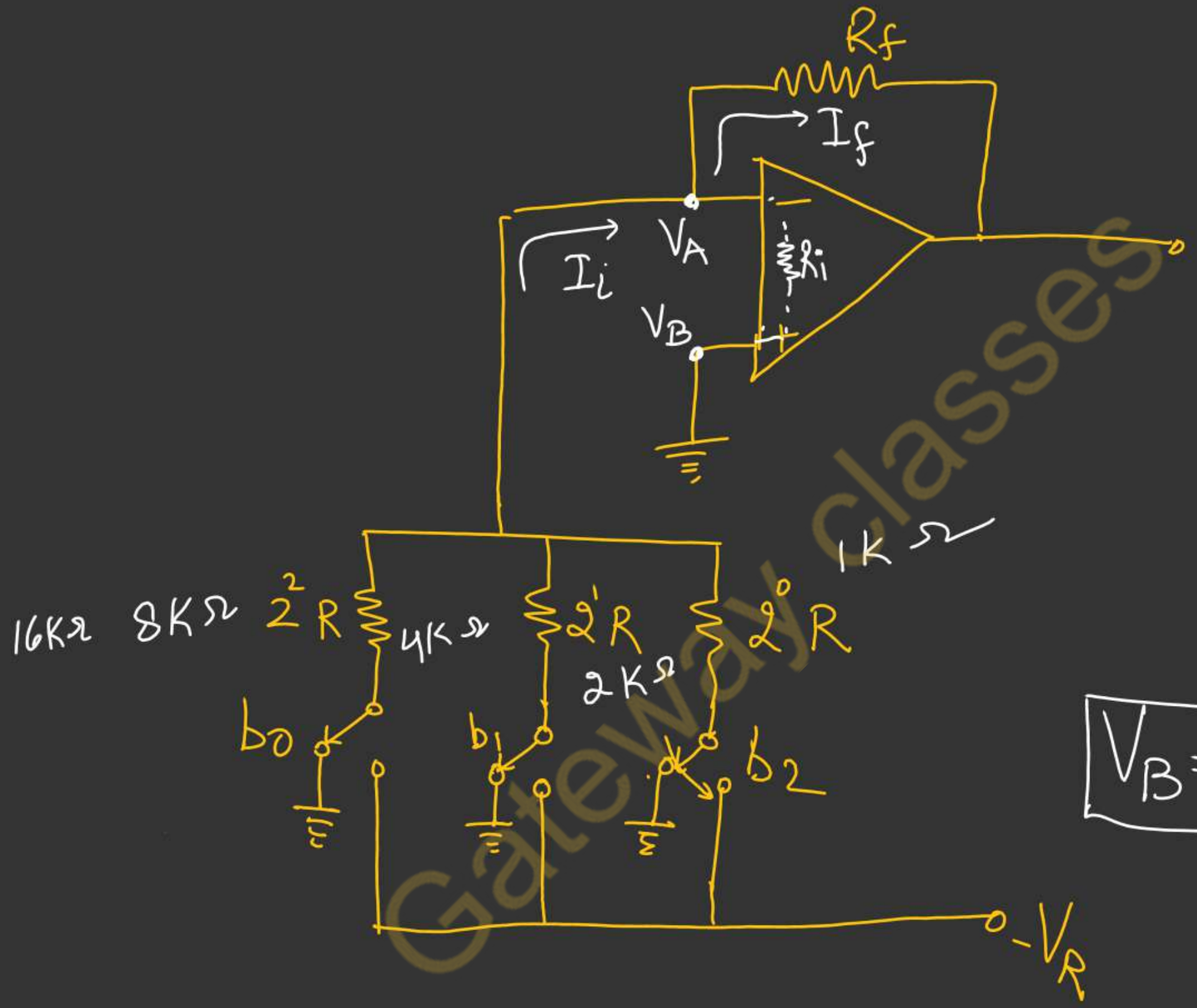
Gateway classes

Weighted Resistor DAC

- A weighted resistor DAC produces an analog output, which is almost equal to the digital (binary) input by using binary weighted resistors in the inverting adder circuit.
- The circuit diagram of a 3-bit binary weighted resistor DAC is shown in the following figure.



Gateway classes



$$A_d = V_B - V_A$$

$$\frac{V_B - V_A}{A_d} = 0$$

$$V_B - V_A = 0$$

$$V_B = V_A$$

$$V_B = 0V \;;\; V_A = 0V$$ VGC

Gateway classes

$$I_i = I_f$$

$$\frac{V_A-(-V_R)b_2}{2^0R}+\frac{V_A-(-V_R)b_1}{2^1R}+\frac{V_A-(-V_R)b_0}{2^2R}$$

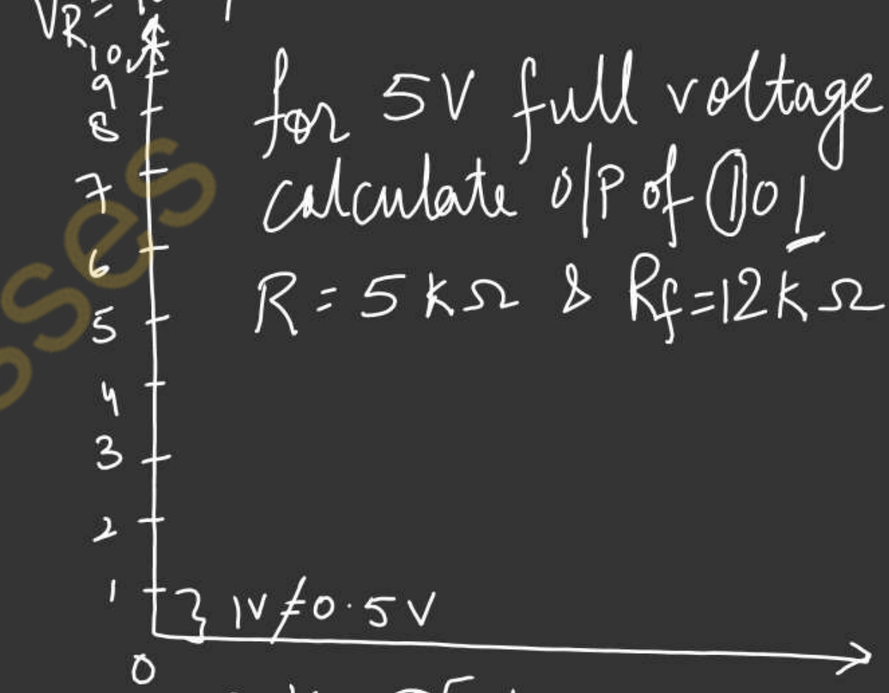
$$=\frac{V_0-V_A}{R_f}$$

$$\frac{V_R b_2}{2^0R}+\frac{V_R b_1}{2^1R}+\frac{V_R b_0}{2^2R}=\frac{V_0}{R_f}$$

$$\boxed{V_0=\frac{R_f}{R}\cdot V_R\left[\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right]}$$ ✓

If $R=2R_f$

$$\boxed{V_0=\frac{V_R}{2}\left[\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right]}$$



5 V

for 5V full voltage calculate o/p of 101

$R = 5k\Omega$ & $R_f = 12k\Omega$

$$V_0 = \frac{12k}{5k}\times 5\left[\frac{1}{2^0}+\frac{0}{2^1}+\frac{1}{2^2}\right]$$

$$= 12\left[1+0+\frac{1}{8}\right]$$

$$= 12\left[\frac{1}{2}+0+0.25\right]$$

$$= (12\times 1.25)$$

Gateway classes

- Let the 3-bit binary input is b2b1b0 with b2 = MSB & b0 = LSB
- The digital switches will be connected to ground, when the corresponding input bits are equal to '0'.
- The digital switches will be connected to the negative reference voltage, −VR when the corresponding input bits are equal to '1'.
- The non-inverting input terminal of an op-amp is connected to ground. That means zero volts is applied at the non-inverting input terminal of op-amp.
- According to the virtual short concept, the voltage at the inverting input terminal of op-amp is same as that of the voltage present at its non-inverting input terminal.
- So, the voltage at the inverting input terminal's node will be zero volts.

Gateway classes

Disadvantages of a binary weighted resistor DAC

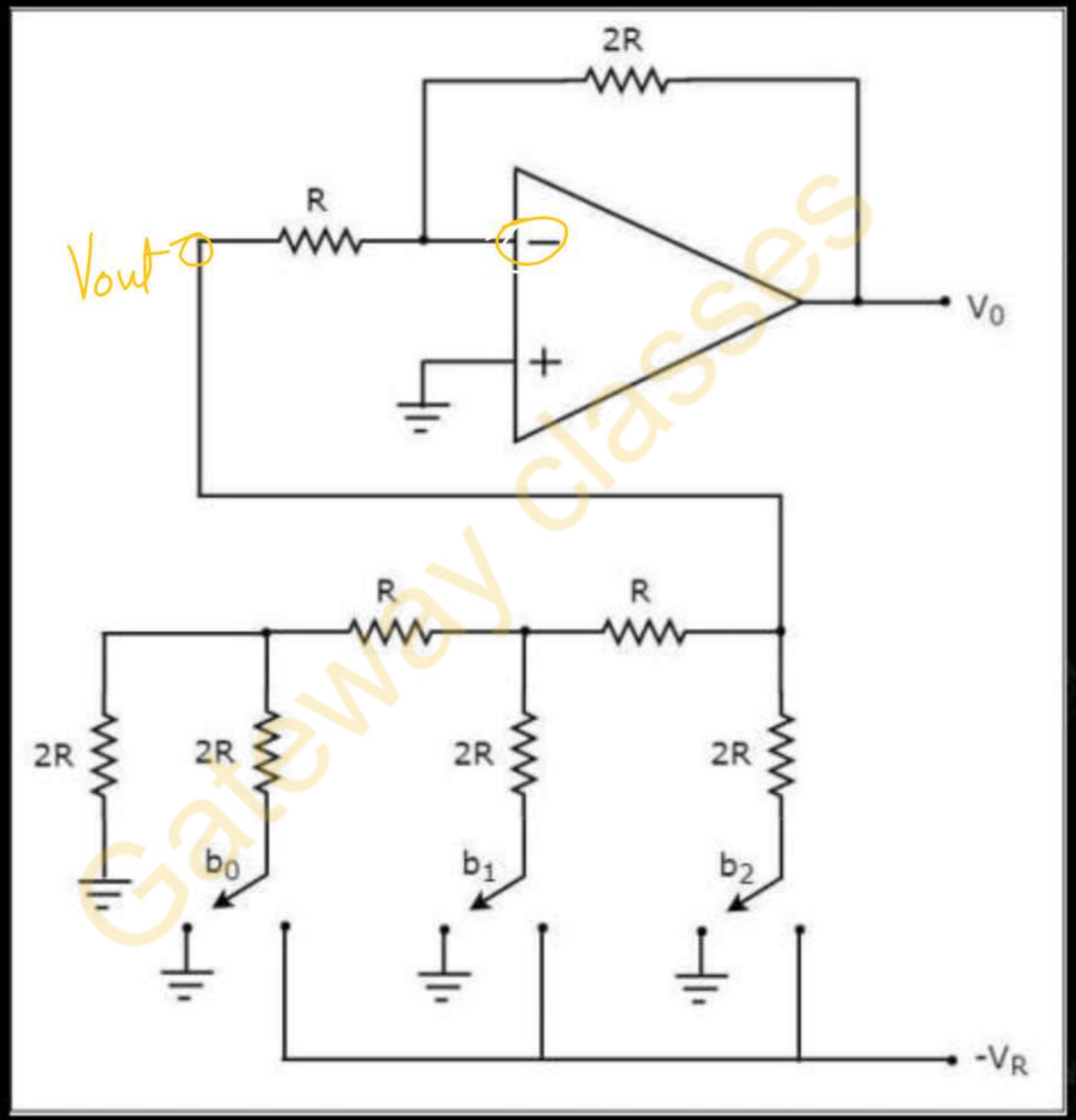
- The difference between the resistance values corresponding to LSB & MSB will increase as the number of bits present in the digital input increases.
- It is difficult to design more accurate resistors as the number of bits present in the digital input increases.

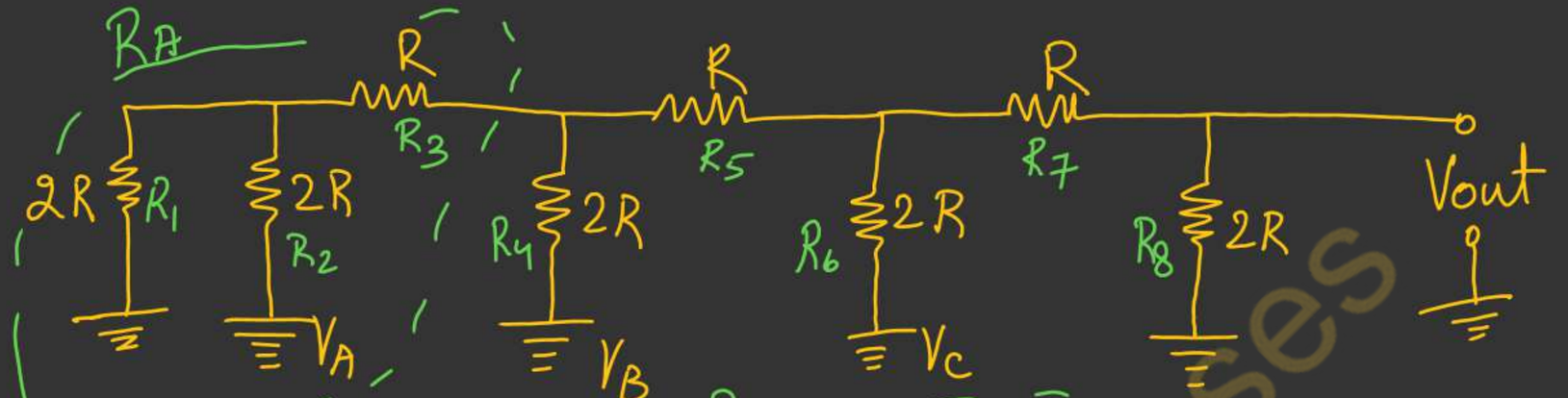
Gateway classes

R-2R Ladder DAC

- It overcomes the disadvantages of a binary weighted resistor DAC.
- R-2R Ladder DAC produces an analog output, which is almost equal to the digital (binary) input by using a R-2R ladder network in the inverting adder circuit.

Gateway classes


2R
R
Vout
V_0
R
R
2R
2R
2R
2R
b_0
b_1
b_2
$-V_R$



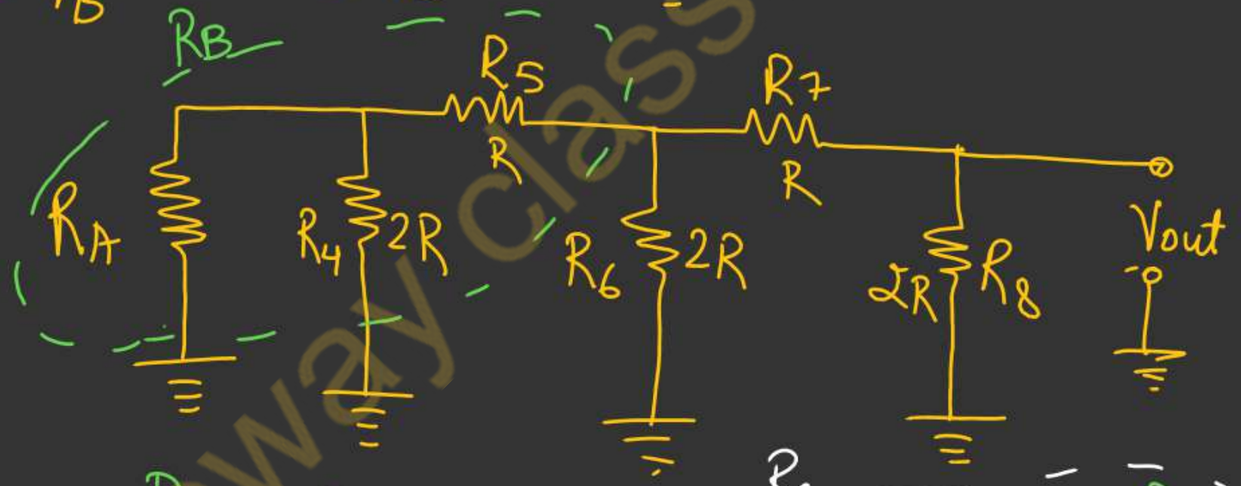
Bit = 0000

$$R_A = \frac{R_1 R_2}{R_1 + R_2} + R_3$$

$$= \frac{2R + 2R}{2R + 2R} + R$$

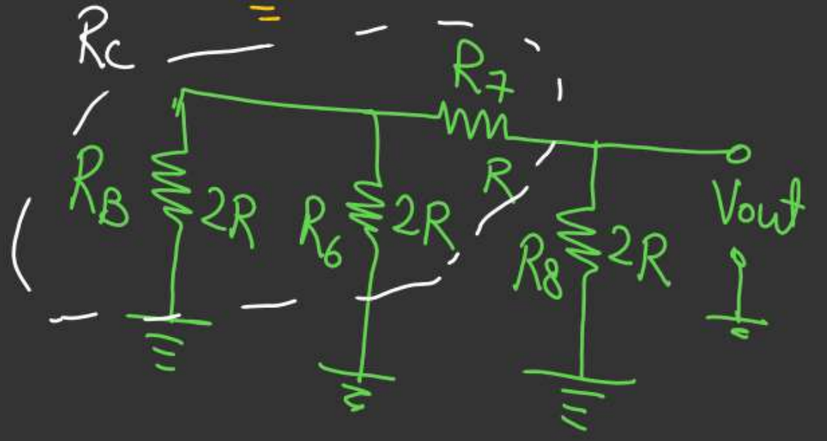
$$= \frac{4R^2}{4R} + R$$

$$R_A = 2R$$



$$R_B = \frac{R_A R_4}{R_A + R_4} + R_5$$

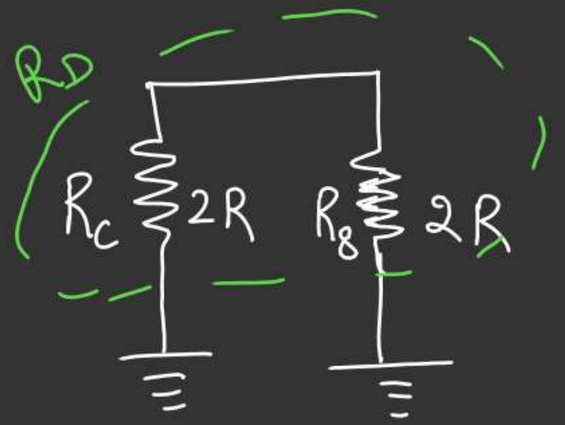
$$R_B = 2R$$



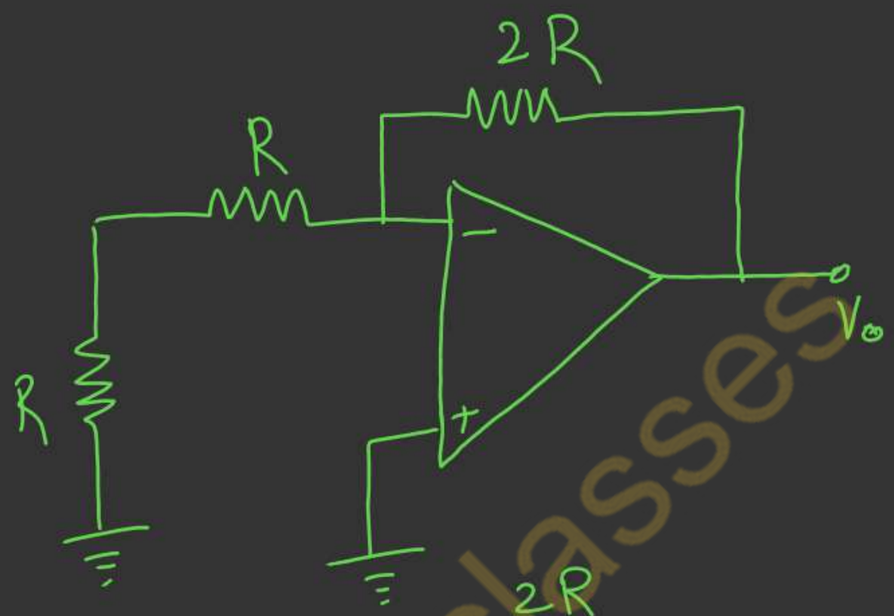
Gateway classes

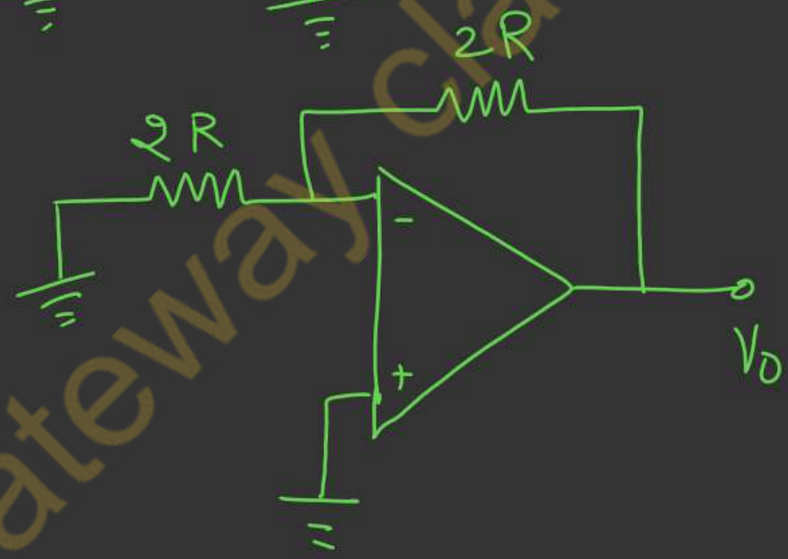
$$R_C = \frac{R_B R_6}{R_B + R_6} + R_7$$

$$= 2R$$



$$R_D = R$$





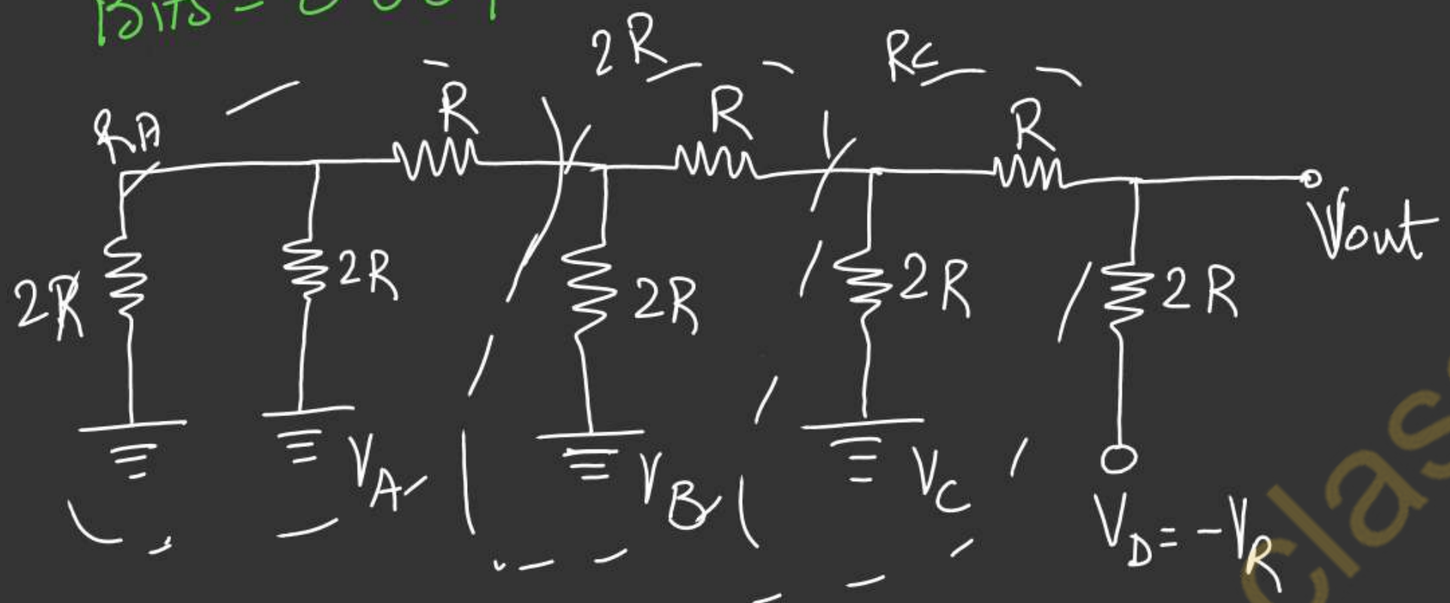
$$V_0 = \frac{R_f}{R} V_{in}$$

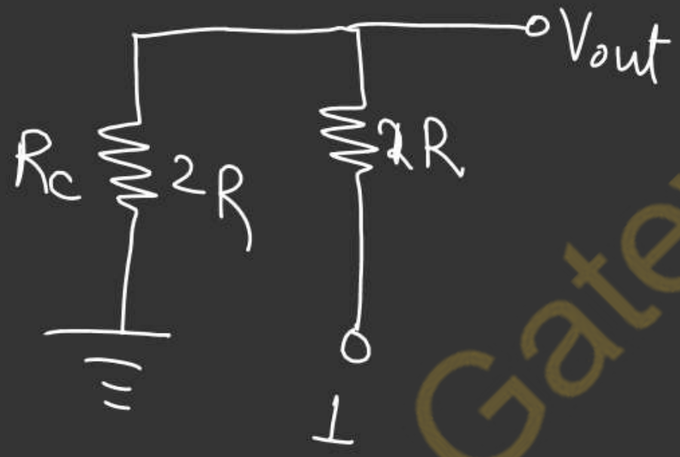
$$= \frac{2R}{2R} \times V_{in}$$

$$= 0\ V$$

Gateway classes

Bits = 0 0 0 1





$V_R = 5V$

$V_{out} = \frac{5V}{16} \times 1 = 0.3125\ V$

$= 312.5\ mV$

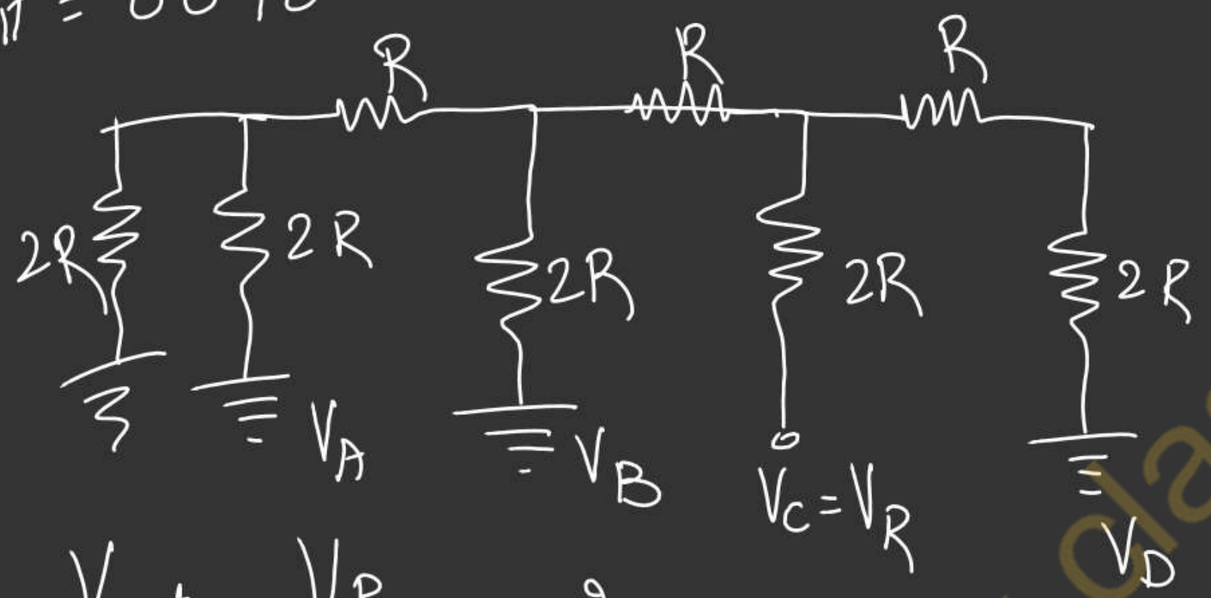
$V_R = 10V$

$V_{out} = \frac{10}{16} \times 1$

$=$

Gateway classes

bit = 0010



$$V_{out} = \frac{V_R}{16} \times 2$$

$$= \frac{5\,V}{16} \times 2$$

$$= 625\,mV$$

$$Resolution = \frac{V_R}{2^n}$$

Gateway classes

$n = 9$ bit DAC

000 000 000 = 0 V

111 111 111 = 10.3 V

$^{8}1\ ^{7}0\ ^{6}1\ ^{5}1\ ^{4}0\ ^{3}1\ ^{2}1\ ^{1}1\ ^{0}1$ = ?

$$V_0 = V_R \left[\frac{b^{n-1}}{2^1} + \frac{b^{n-2}}{2^2} + \frac{b^{n-3}}{2^3} + \cdots \frac{b_0}{2^{n-1}} \right]$$

$$= 10.3 \left[\frac{1}{2^1} + \frac{0}{2^2} + \frac{1}{2^3} + \frac{1}{2^4} + \frac{0}{2^5} + \frac{1}{2^6} + \frac{1}{2^7} + \frac{1}{2^8} + \frac{1}{2^9} \right]$$

$$= 7.383 \text{ V}$$

Gateway classes

DIGITAL SYSTEM DESIGN

UNIT 5 : Digital-to-Analog converters (DAC)
Lec 2

Today's Target

- Analog-to-digital converter
- ADC Process
- Types of Analog to Digital Converter
- Application of ADC
- Single Slope ADC
- University Questions

Gateway classes

UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
21-22	Explain single slope and dual slope ADC with a neat sketch.	10 Marks

Gateway classes

Analog-to-digital converter

- An analog-to-digital converter (ADC, A/D, or A-to-D) is a system that converts an analog signal, such as a sound picked up by a microphone or light entering a digital camera, into a digital signal.

- An ADC may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number representing the magnitude of the voltage or current.

- A/D converter is a linkage between the analog (linear) world of transducers and discrete world of processing the signal and handling the data.

Gateway classes

ADC Process

- There are mainly two steps involves in the process of conversion. They are
- 1) Sampling and Holding
- 2) Quantizing and Encoding
- The whole ADC conversion process is shown in figure.

1.10 → 1
1.60 → 2

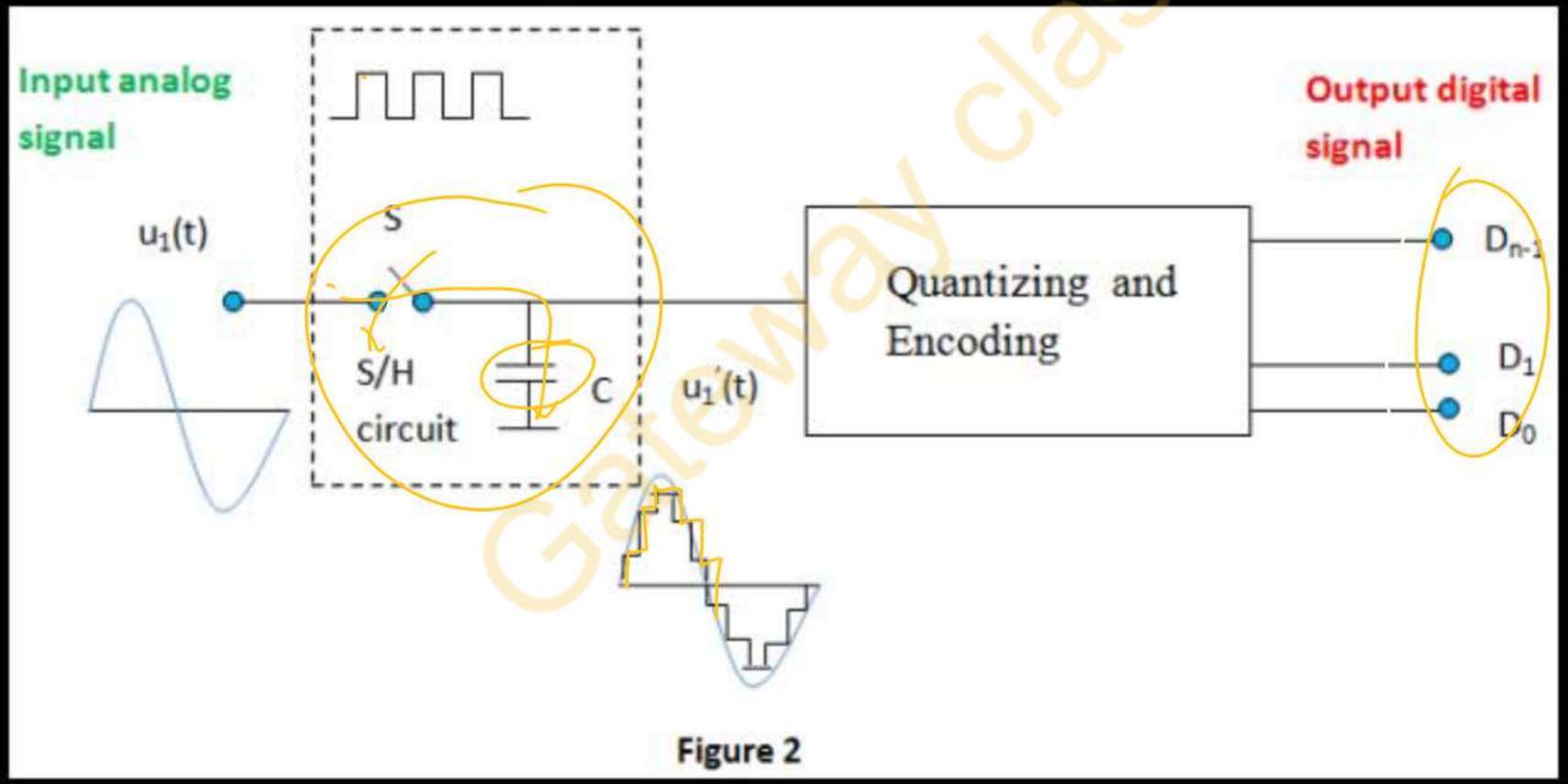
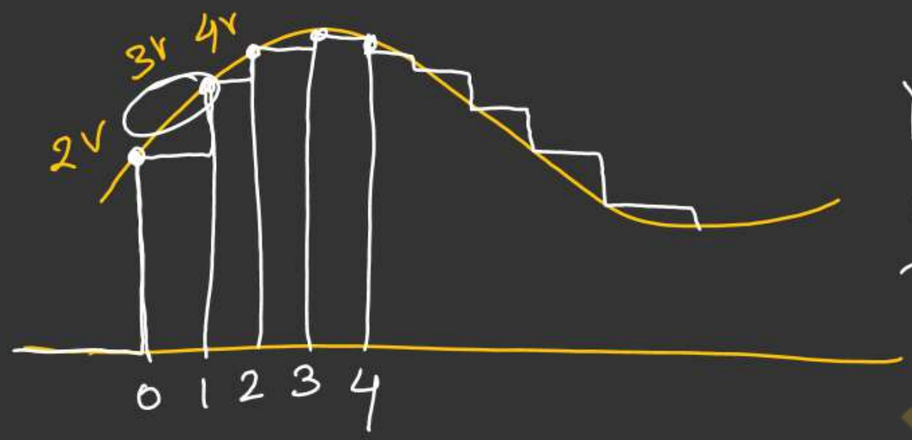


Figure 2

Gateway classes

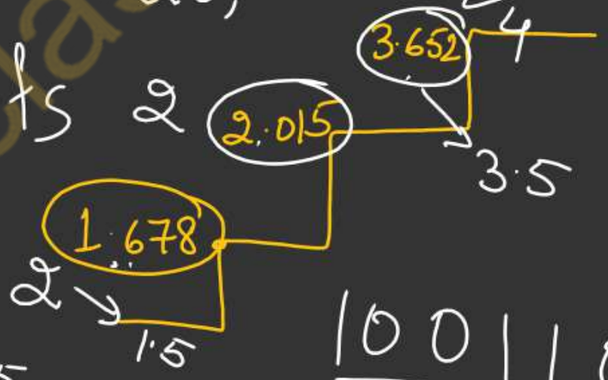


Nyquist Criteria

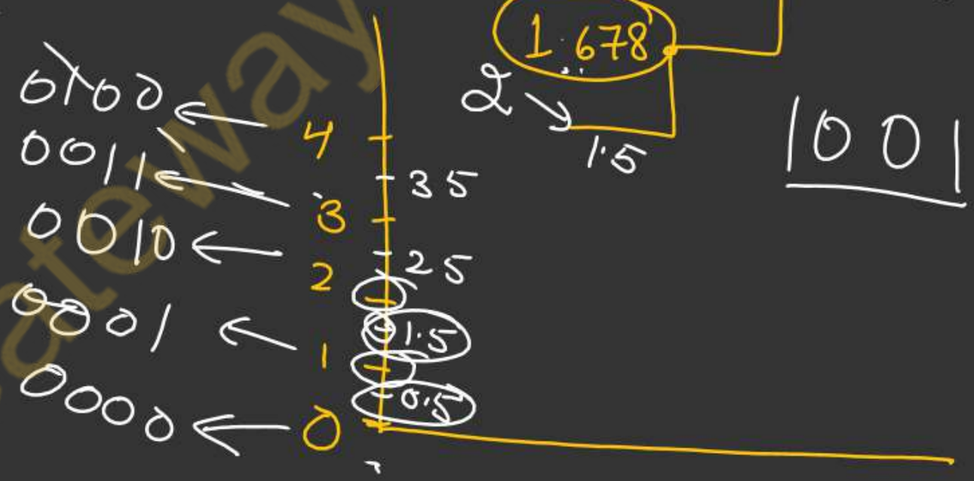
$f_s \geq 2f_m$

20,000 x 2

f_s 2







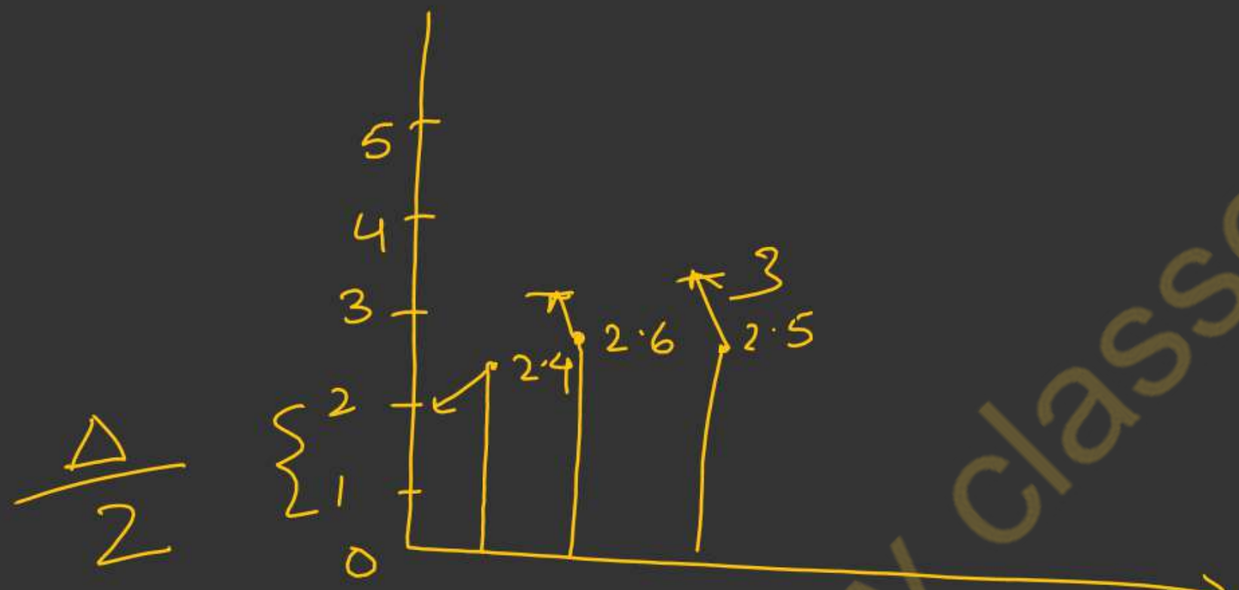
1001 | 011 | 001 | 10

Gateway classes

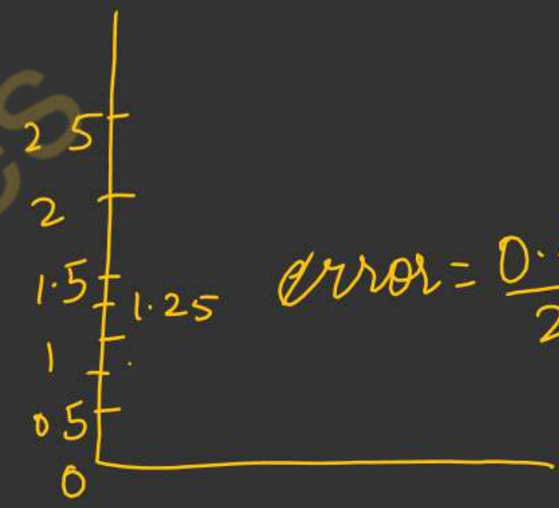
ADC Process

- Sampling and Holding:
- In the process of Sample and hold (S/H), the continuous signal will gets sampled and freeze (hold) the value at a steady level for a particular least period of time.
- It is done to remove variations in input signal which can alter the conversion process and thereby increases the accuracy.
- The minimum sampling rate has to be two times the maximum data frequency of the input signal.
- Quantizing:
- It is the process in which the reference signal is partitioned into several discrete quanta and then the input signal is matched with the correct quantum.
- For understanding quantizing, we can first go through the term Resolution used in ADC.
- It is the smallest variation in analog signal that will result in a variation in the digital output.
- This actually represents the quantization error.
  Resolution $\Delta V = VR / 2^N$
- V → Reference voltage range
  2^N → Number of states

Gateway classes



$\frac{\Delta}{2}$



$error = \frac{0.5}{2} = 0.25$



Gateway classes

Encoding

- For each quantum, a unique digital code will be assigned and after that the input signal is allocated with this digital code.
- The process of quantizing and encoding is demonstrated in the table beside:
- Only one digital value is used to represent the whole range of voltage in an interval.
- Thus, an error will occur and it is called quantization error. This is the noise introduced by the process of quantization.
- The maximum quantization error is: $\pm (1/2)\,\Delta V = \pm 0.5$ V

Analog signal			Digital o/p
7.5	7	7Δ=7V	111
6.5	6	6Δ=6V	110
5.5	5	5Δ=5V	101
4.5	4	4Δ=4V	100
3.5	3	3Δ=3V	011
2.5	2	2Δ=2V	010
1.5	1	1Δ=1V	001
0.5	0	0Δ=0V	000

Gateway classes

Types of Analog to Digital Converter

- Successive Approximation ADC: This converter compares the input signal with the output of an internal DAC at each successive step. It is the most expensive type.
- Dual Slope ADC: It have high accuracy but very slow in operation.
- Pipeline ADC: It is same as that of two step Flash ADC.
- Delta-Sigma ADC: It has high resolution but slow due to over sampling.
- Flash ADC: It is the fastest ADC but very expensive.
- Other: Staircase ramp, Voltage-to-Frequency, Switched capacitor, tracking, Charge balancing, and resolver.

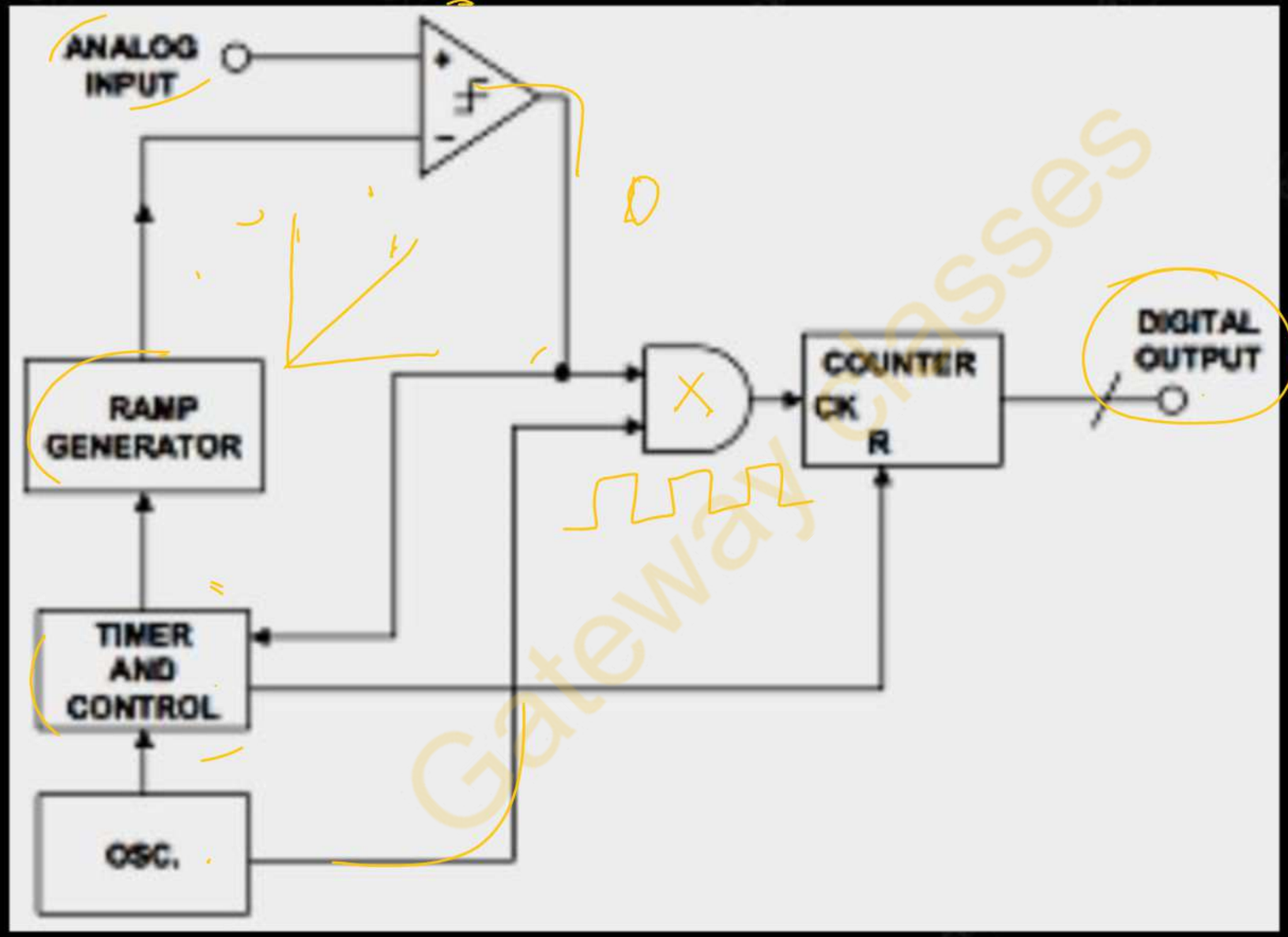
Gateway classes

Application of ADC

- Used together with the transducer.
- Used in computer to convert the analog signal to digital signal.
- Used in cell phones.
- Used in microcontrollers.
- Used in digital signal processing.
- Used in digital storage oscilloscopes.
- Used in scientific instruments.
- Used in music reproduction technology etc.

Gateway classes

SINGLE SLOPE ADC



Gateway classes

WORKING

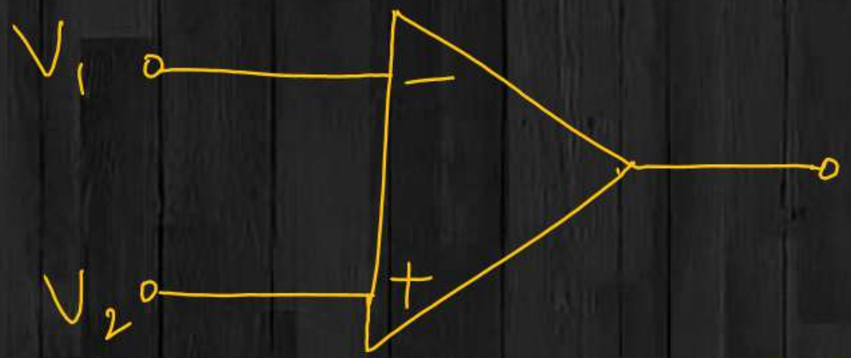
- As soon as input appears, comparator gives positive pulse.
- This pulse triggers AND gate which triggers counter. Counter starts counting.
- Comparator also triggers timer and control which triggers ramp generator.
- Ramp generator generates constant slope ramp signal until the time this ramp exceeds input signal.
- As soon as ramp signal > analog input, comparator generates negative pulse and closes AND gate, stops counter, stops timer and ramp generator.
- The count obtained by counter equals the value of analog input signal.

Gateway classes

Problems in Single Slope ADC

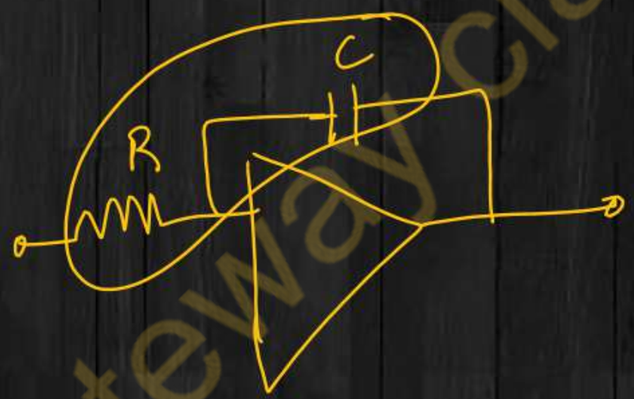
- single-slope A/D can only measure voltages whose sign differs from that of the reference voltage.
- The values of resistors and capacitors are more problematic while dealing with accuracy of the circuit.
- Vsignal being measured ≈ −Vref *Ts *n /RC.
- Thus, n is proportional to the voltage being measured, and n is the digital output of the A/D.

Gateway classes



$V_1 > V_2 \Rightarrow 0$

$V_2 > V_1 \Rightarrow 1$







Gateway classes

DIGITAL SYSTEM DESIGN

UNIT 5 : Digital-to-Analog converters (DAC)

Lec 3

Today's Target

- Dual Slope type ADC
- **Successive-approximation ADC**
- University Questions

Gateway classes

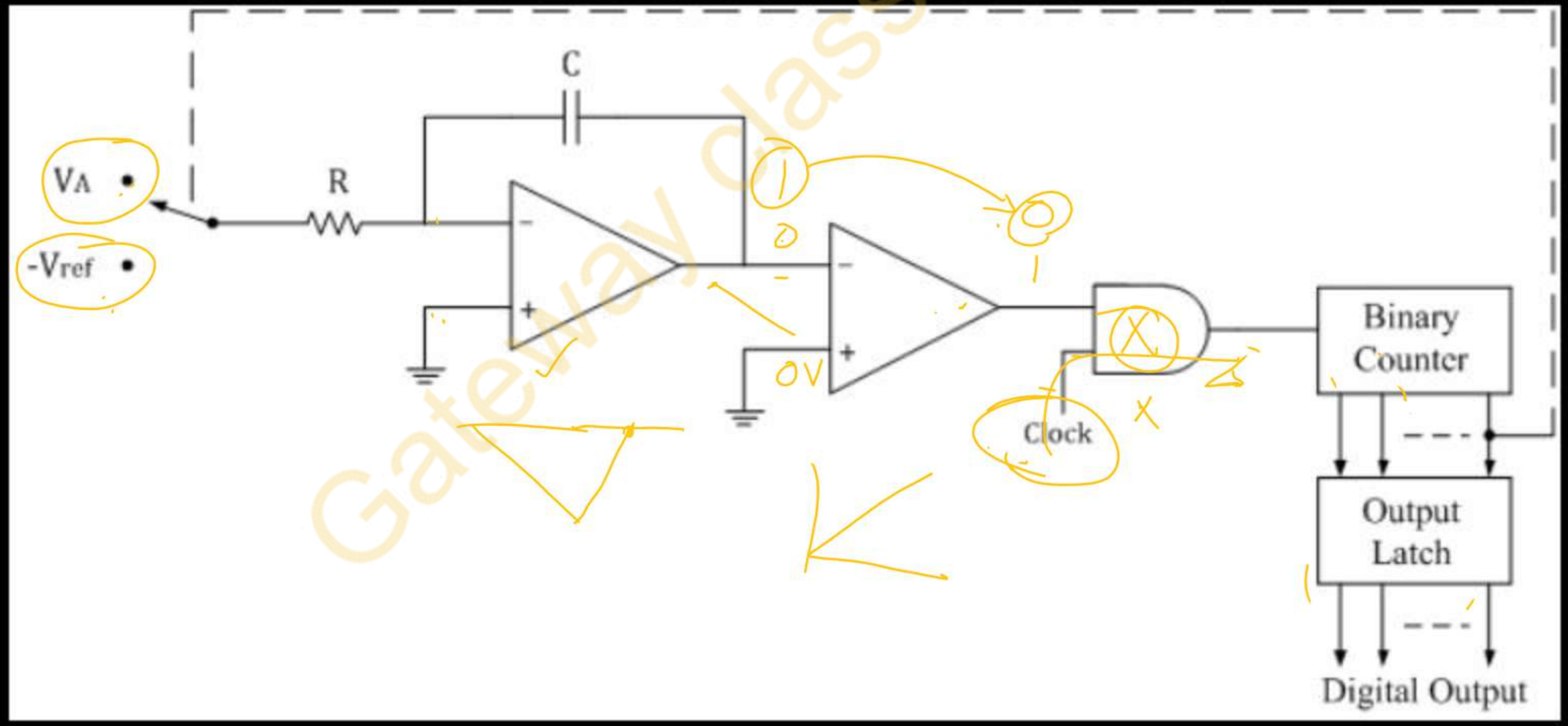
UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
22-23	Draw and explain the dual slope analog to digital convertor	10 Marks
21-22	Explain single slope and dual slope ADC with a neat sketch.	10 Marks
21-22	List some advantages of successive approximation?	2 Marks
21-22	Where is SAR ADC used?	2 Marks
20-21 19-20	Explain the operation of successive approximation ADC. Discuss it merits and demerits.	10 Marks

Gateway Classes

Dual Slope type ADC

- In dual slope type ADC, the integrator generates two different ramps, one with the known analog input voltage VA and another with a known reference voltage –Vref. Hence it is called as dual slope A to D converter.
- The logic diagram for the same is shown below.



Gateway classes

Operation

- The binary counter & output of integrator is initially reset to 0000 i.e. 0V
- The input to the ramp generator or integrator is switched to the unknown analog input voltage V_A which generates a negative ramp output.
- The output of comparator is positive and the clock is passed through the AND gate resulting in counting up of the binary counter.
- The negative ramp continues for a fixed time period t_1, determined by a count detector and generates ramp output given by; $V_S = - V_A / RC \times t_1$
- When the counter reaches the fixed count at time period t_1, the binary counter resets to 0000 and switches the integrator input to a negative reference voltage –Vref.
- Now the ramp generator starts with the initial value –Vs and increases in positive direction until it reaches 0V and the counter gets advanced.
- When Vs reaches 0V, comparator output becomes negative (i.e. logic 0) and the AND gate is deactivated. Hence no further clock is applied through AND gate.
- Now, the conversion cycle is said to be completed and the positive ramp voltage is given by; $V_S = Vref/RC \times t_2$
- Where Vref & RC are constants and time period t_2 is variable.

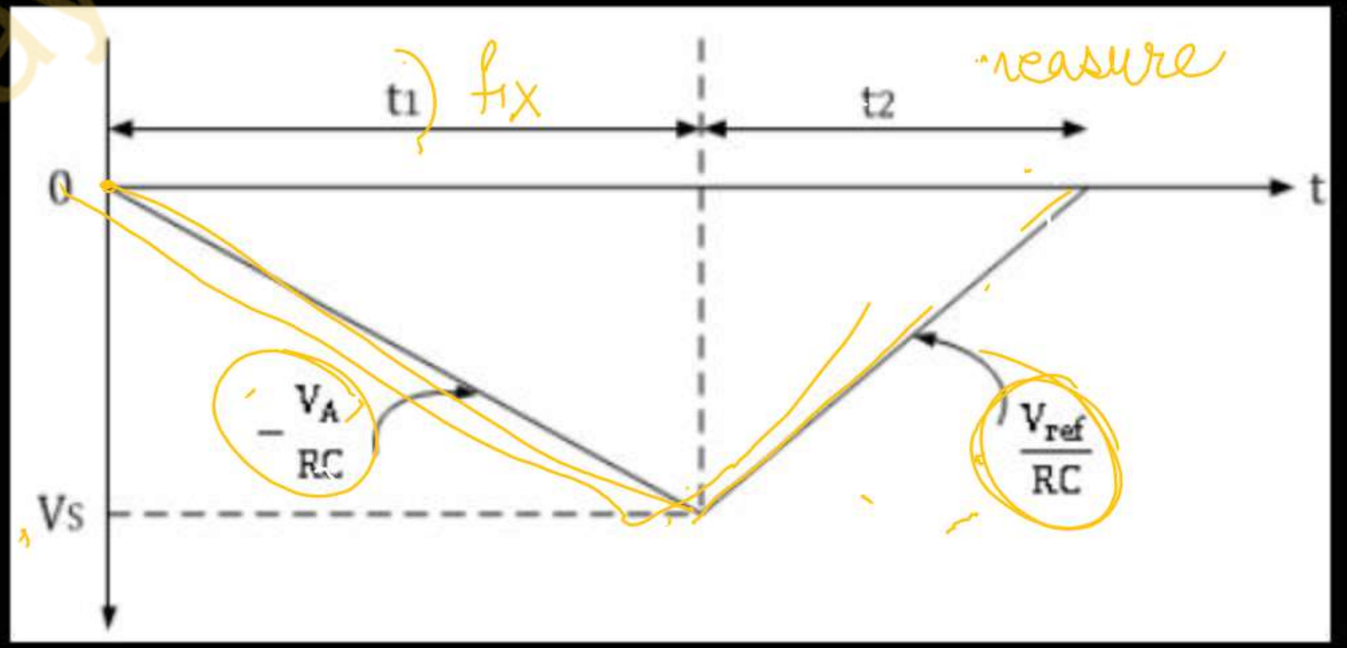
Gateway Classes

The dual ramp output waveform

- Since ramp generator voltage starts at 0V, decreasing down to –Vs and then increasing up to 0V, the amplitude of negative and positive ramp voltages can be equated as follows.
  $\therefore Vref/RC \times t_2 = -VA/RC \times t_1$
  $\therefore t_2 = -t_1 \times V_A / Vref$
  $\therefore V_A = - Vref \times t_2 / t_1$

$V_A \propto t_2$

- Thus the unknown analog input voltage V_A is proportional to the time period t_2, because Vref is a known reference voltage and t_1 is the predetermined time period.
- The binary counter gives corresponding digital value for time period t_2.
- Thus the counter counts digital output as
  Digital output=(counts/sec) t_2
  ∴ Digital output= (counts/sec) $[t_1 \times V_A / Vref]$



Gateway classes

$$-\frac{V_A}{RC} \times t_1 = \frac{V_{ref}}{RC} \times t_2$$

$$V_A = -V_{ref} \times \frac{t_2}{t_1}$$

Gateway Classes

For example

- Consider;
- the clock frequency is 1 MHz,
- the reference voltage is -1V,
- the fixed time period t1 is 1ms and
- the RC time constant is also 1 ms.
- Assuming the unknown analog input voltage amplitude as $V_A = 5V$,
- during the fixed time period t1 , the integrator output Vs is;

$$V_S = - V_A /RC \times t_1 = (-5)/1ms \times 1ms = - 5V$$

- During the time period t_2, ramp generator will integrate all the way back to 0V.

$$\therefore t_2 = V_S /Vref \times RC = (-5)/(-1) \times 1ms = 5ms = 5000\mu s$$

- Hence the 4-bit counter value is 5000
- By activating the decimal point of MSD seven segment displays, the display can directly read as 5V.

$$V_S = -\frac{V_A}{RC} \times t_1 = -\frac{5}{1ms} \times 1ms$$

$$V_S = -5$$

$$= -\frac{V_{ref}}{RC} \times t_2 = \frac{-1}{1ms} \times t_2$$

$$-5 = \frac{-1}{1ms} \times t_2$$

$$-5ms = -t_2$$

$$t_2 = 5ms$$

Gateway classes

Successive-approximation ADC

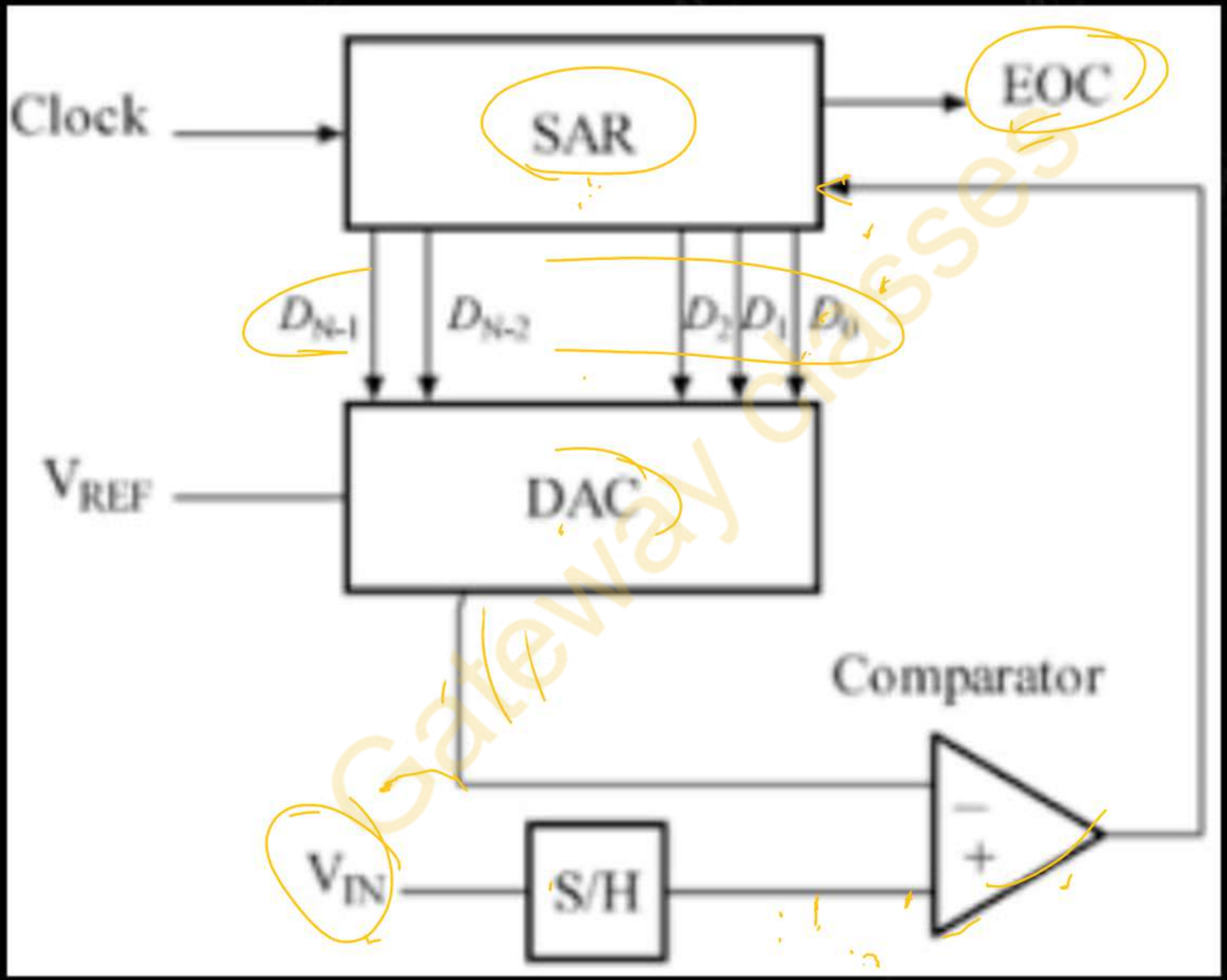
- A successive-approximation ADC is a type of ADC that uses a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.
- The only change in this design is a very special counter circuit known as a successive-approximation register. (SAR)



- This register counts by trying all values of bits starting with the most-significant bit and finishing at the least-significant bit.
- Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly.
- The way the register counts is identical to the "trial-and-fit" method
- The advantage to this counting strategy is much faster results.

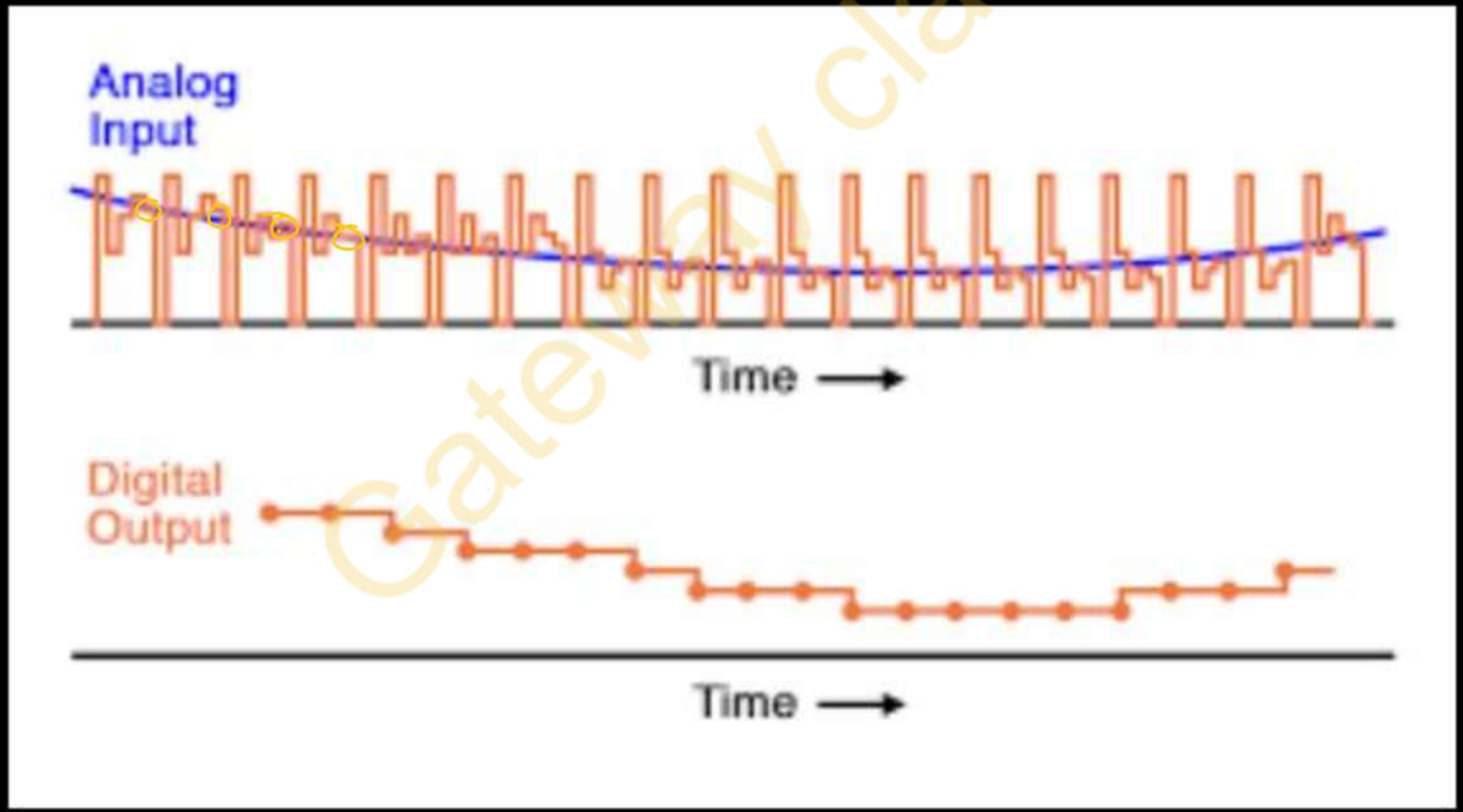
Gateway classes

Successive-approximation ADC



Gateway Classes

- SAR is generally capable of outputting the binary number in serial (one bit at a time) format, thus eliminating the need for a shift register.
- Plotted over time, the operation of a successive-approximation ADC looks like this:



Gateway classes

DIGITAL SYSTEM DESIGN

UNIT 5 : Digital-to-Analog converters (DAC)

Lec 4

Today's Target

- Flash ADC with and without Priority Encoder
- Advantages and Disadvantages of flash type ADC
- Switched Capacitor
- switched-capacitor resistor and its application
- Switched-Capacitor Circuit Advantages
- University Questions

Gateway classes

UNIVERSITY QUESTIONS

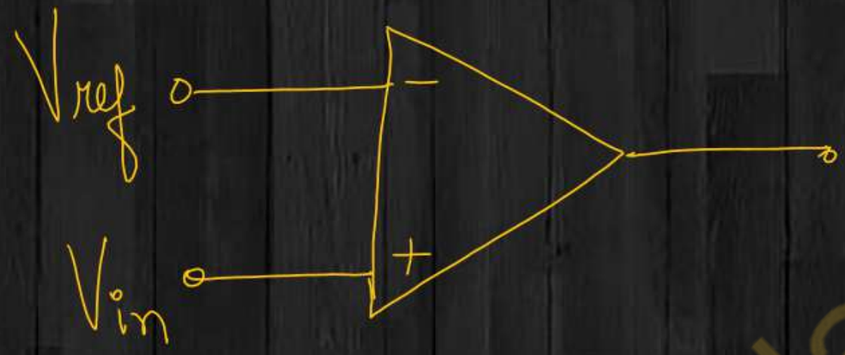
YEAR	QUESTIONS	MARKS
22-23 19-20	What are the advantages and disadvantages of flash type ADC	2 Marks
21-22	Describe switched capacitor and write its applications.	10 Marks
20-21 19-20	With a neat sketch Explain the operation of FLASH ADC.	10 Marks

Gateway classes

Flash ADC

- Also called the parallel A/D converter
- It is formed of a series of comparators, each one comparing the input signal to a unique reference voltage.
- The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output.
- Vref is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit.
- As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state.
- The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.

Gateway classes



$V_{ref} > V_{in} \Rightarrow$ logic 0

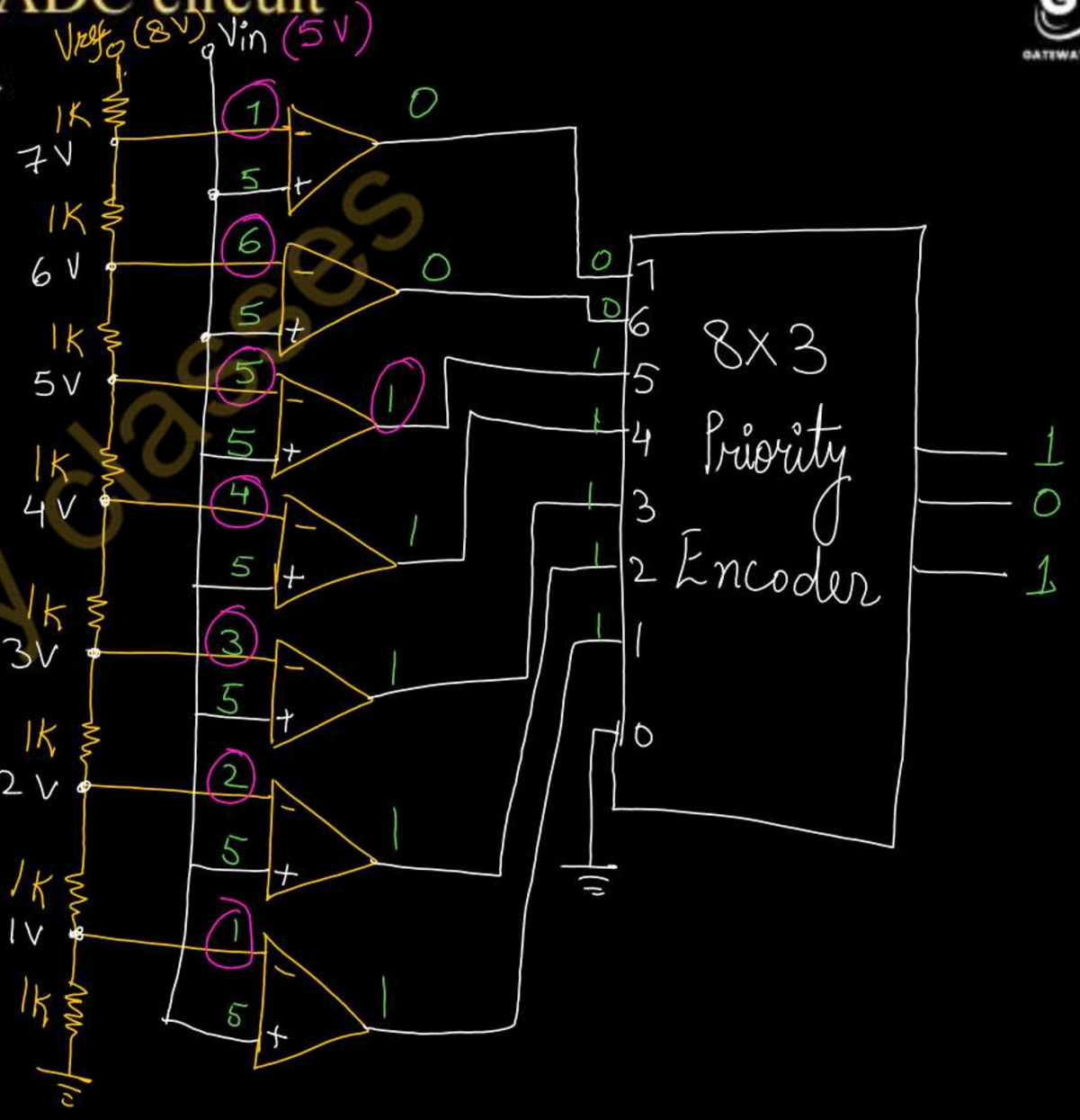
$V_{ref} < V_{in} \Rightarrow$ logic 1

$V_{ref} = V_{in} \Rightarrow$ logic 1

Gateway classes

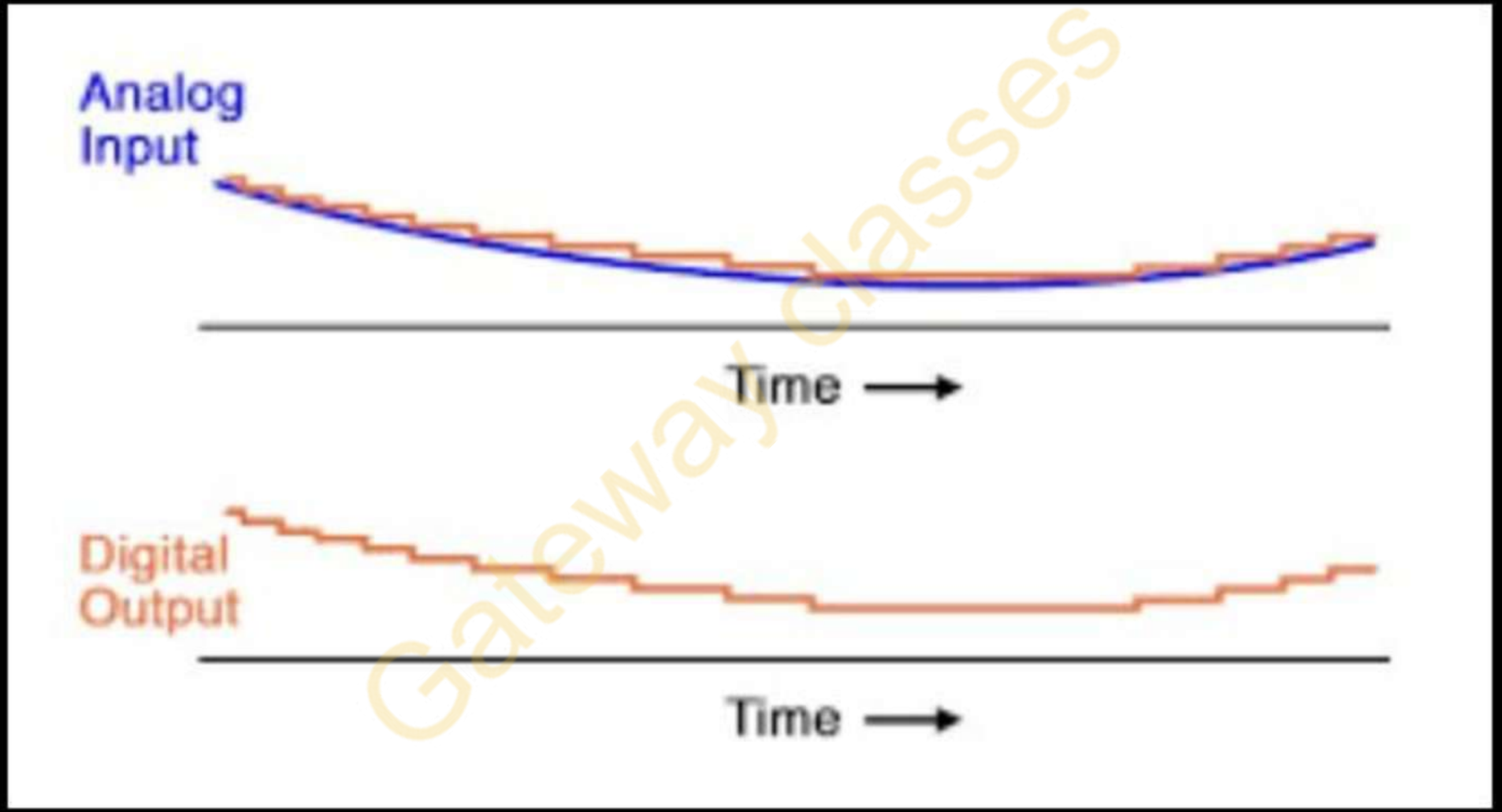
3-bit flash ADC circuit

- The logic diagram for the same is shown below.



Gateway Classes

Output of Flash ADC



Gateway classes

Flash ADC without Priority Encoder

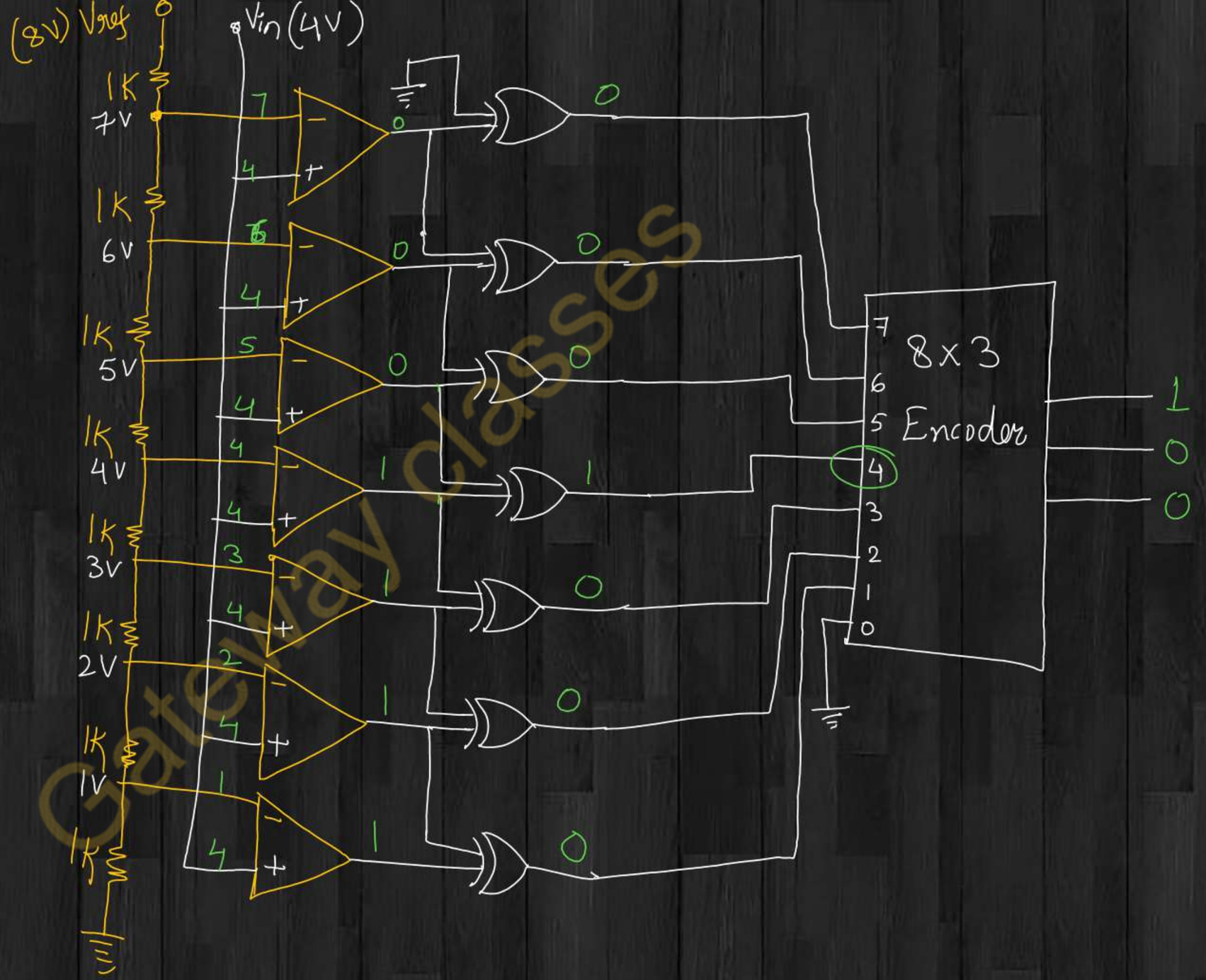
- For this particular application, a regular priority encoder with all its inherent complexity isn't necessary.
- Due to the nature of the sequential comparator output states (each comparator saturating "high" in sequence from lowest to highest), the same "highest-order-input selection" effect may be realized through a set of Exclusive-OR gates, allowing the use of a simpler, non-priority encoder:

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Ex-OR

$Y = \bar{A}B + A\bar{B}$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



Gateway classes

Advantages and Disadvantages of flash type ADC

- Flash ADCs offer many advantages such as high speed and low latency.
- They also have some drawbacks such as high power consumption, large size, and limited resolution.
- These drawbacks can be mitigated by using sub-ranging or folding architectures, as well as interpolation techniques

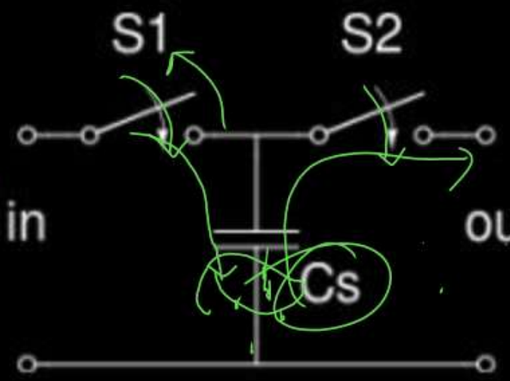
Gateway classes

Switched Capacitor

- A switched capacitor (SC) is an electronic circuit element implementing a filter.
- It works by moving charges into and out of capacitors when switches are opened and closed.
- Usually, non-overlapping signals are used to control the switches, so that not all switches are closed simultaneously.
- This makes them much more suitable for use within integrated circuits, where accurately specified resistors and capacitors are not economical to construct.

Gateway classes

The switched-capacitor resistor



- The simplest switched-capacitor (SC) circuit is the switched-capacitor resistor, made of one capacitor C and two switches S_1 and S_2 which connect the capacitor with a given frequency alternately to the input and output of the SC.
- Each switching cycle transfers a charge q from the input to the output at the switching frequency f.
- The charge *q* on a capacitor *C* with a voltage *V* between the plates is given by: $q = CV$
- where *V* is the voltage across the capacitor.
- Therefore, when S_1 is closed while S_2 is open, the charge stored in the capacitor C_S is: $q_{IN} = C_S V_{IN}$
- When S_2 is closed (S_1 is open - they are never both closed at the same time), some of that charge is transferred out of the capacitor, after which the charge that remains in capacitor C_S is: $q_{OUT} = C_S V_{OUT}$

Gateway Classes

The switched-capacitor resistor

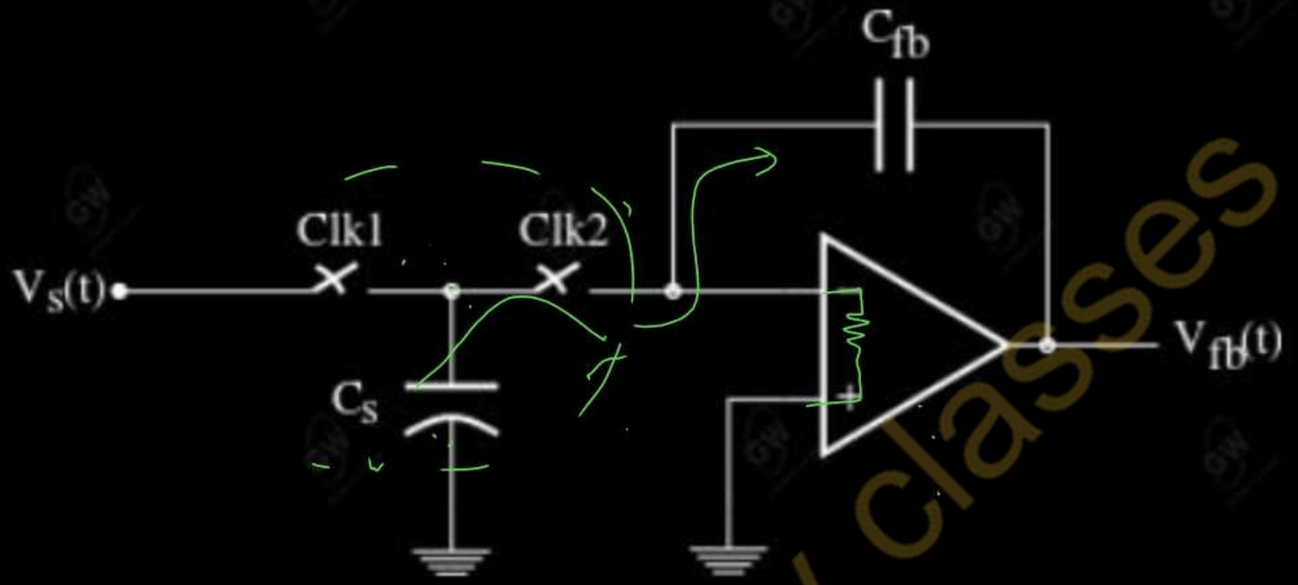
- Thus, the charge moved out of the capacitor to the output is: $q = q_{IN} - q_{OUT} = C_S [V_{IN} - V_{OUT}]$
- Since this charge q is transferred at a rate f, the rate of transfer of charge per unit time is: $I = qf$
- A continuous transfer of charge from one node to another is equivalent to a current, so

  $$I = C_S [V_{IN} - V_{OUT}] f$$

- Let V be the voltage across the SC from input to output. So: $V = V_{IN} - V_{OUT}$
- So the equivalent resistance R (i.e., the voltage–current relationship) is: $R = V/I = 1/(C_S f)$
- Thus, the SC behaves like a resistor whose value depends on capacitance C_S and switching frequency f.
- The SC resistor is used as a replacement for simple resistors in integrated circuits because it is easier to fabricate reliably with a wide range of values.
- It also has the benefit that its value can be adjusted by changing the switching frequency (i.e., it is a programmable resistance).

Gateway classes

The parasitic-sensitive integrator



- Often switched-capacitor circuits are used to provide accurate voltage gain and integration by switching a sampled capacitor onto an op-amp with a capacitor C_{fb} in feedback.
- One of the earliest of these circuits is the parasitic-sensitive integrator developed by the Czech engineer Bedrich Hosticka.

Gateway classes

- In capacitors, charge = capacitance × voltage
- when S1 opens and S2 closes we have the following:

$q = cV$

  - Because C_S has just charged: $Q_S(t) = C_S \cdot V_S(t)$
  - Because the feedback cap, C_{fb}, is suddenly charged with that much charge (by the op amp, which seeks a virtual short circuit between its inputs): $Q_{fb}(t) = Q_S(t-T) + Q_{fb}(t-T)$
  - Now dividing 2) by C_{fb}: $V_{fb}(t) = [Q_S(t-T)/C_{fb}] + V_{fb}(t-T)$
  - And inserting 1): $V_{fb}(t) = [C_S / C_{fb}]V_S(t-T) + V_{fb}(t-T)$
  - This last equation represents what is going on in C_{fb} - it increases (or decreases) its voltage each cycle according to the charge that is being "pumped" from C_S (due to the op-amp).
  - However, there is a more elegant way to formulate this fact if T is very short.
  - Let us introduce $dT \leftarrow T$ and $dV_{fb} \leftarrow V_{fb}(t) - V_{fb}(t-T)$ and rewrite the last equation divided by dt: $dV_{fb}(t)/dt = f[C_S / C_{fb}]^* V_S(t)$
  - Therefore, the op-amp output voltage takes the form:
  - $V_{OUT}(t) = -V_{fb}(t) = -[1/\{(1/f C_S) * C_{fb}\}]^* \int V_S(t)dt$
  - This is an inverting integrator with an "equivalent resistance $R_{eq} = 1/f C_S$
  - This allows its *on-line* or *runtime* adjustment.

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Switched-Capacitor Circuit Advantages

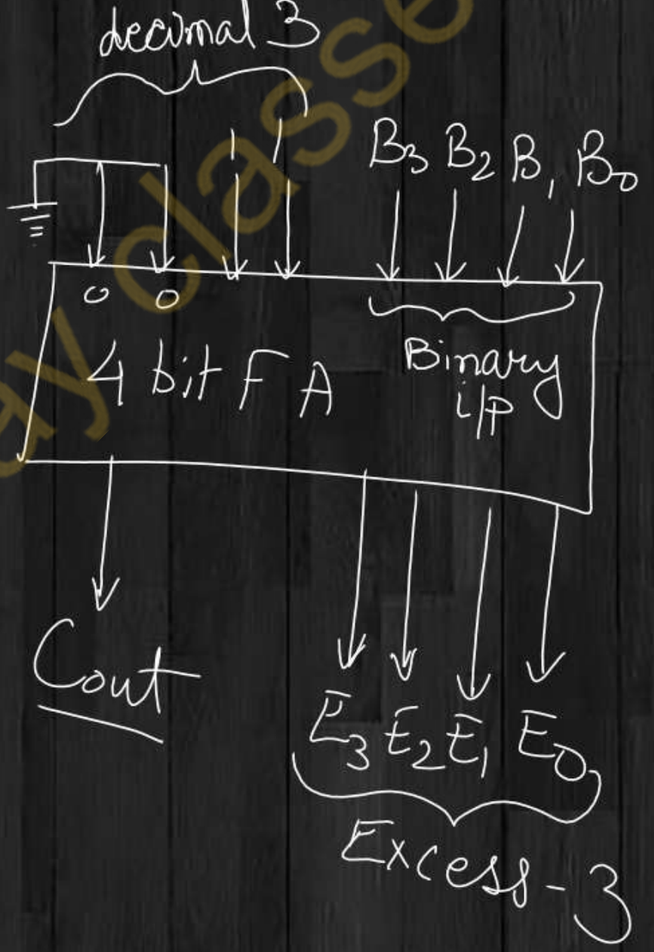
- Saves space while achieving high resistance values.
- Achieve a frequency response accuracy of the order of 0.1%.
- Matching similar IC components(such as capacitor to capacitor) instead of two different components(such as capacitor to resistor) allows for this level of precision.
- Easier to reliably implement with a broader range of values, making it an ideal replacement for traditional resistors in any integrated circuit application.
- Possible to adjust the equivalent resistor value by changing the clock speed.

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Binary to Excess-3 using FA

Bin + 0011 $\Rightarrow$ Excess 3

dec 3



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