AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-3 Lec-1



Avinash Sir

Today's target

- Introduction to Sequential Circuits
- SR Latch ,D Latch
- PYQ

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

Sequential Circuits

Sequential circuits are a type of digital circuit where the output depends not only on the current inputs but also on the history of past inputs, which is stored as the circuit's state. They rely on feedback loops to retain information about previous states. They are widely used in systems requiring memory, timing, or sequential operations, such as counters, registers, and finite state machines.

Key Characteristics of Sequential Circuits:

- **Memory Elements:** Sequential circuits include memory components like flip-flops or latches, which store the state of the circuit.
- **Dependence on Past Inputs:** The output is a function of both current inputs and the stored state (past inputs).
- **Clock Signal:** Most sequential circuits are synchronous, meaning they operate in sync with a clock signal.

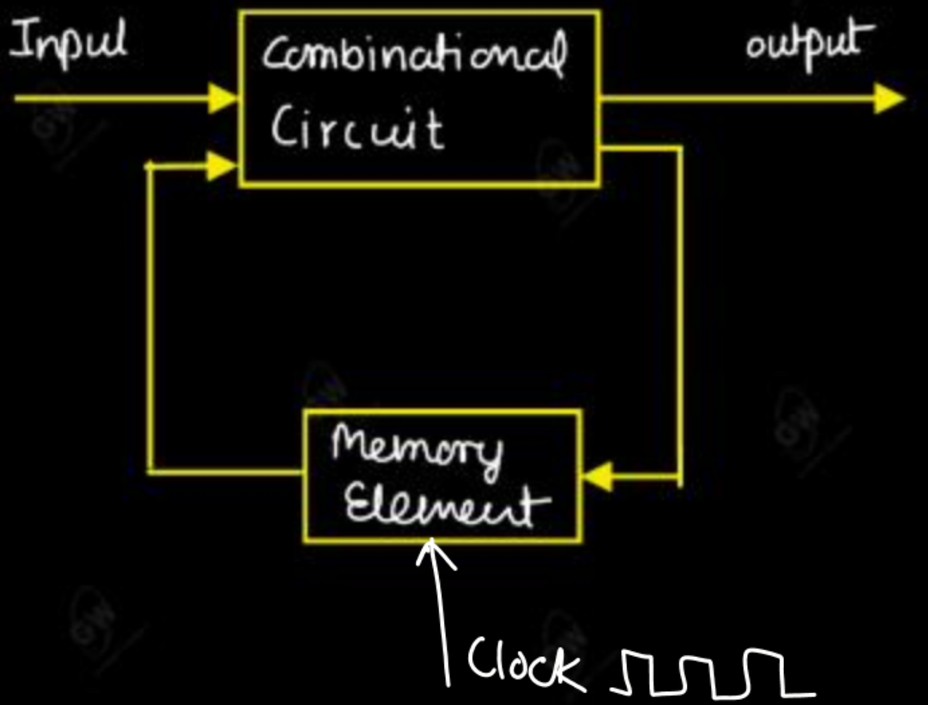
Gateway Classes

Basic Building Blocks of Sequential Circuits

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1. Flip-Flops (Memory Elements): Flip-flops are the fundamental memory units in sequential circuits. They store 1 bit of data (0 or 1). SR, JK, D, T
2. Latches :-Latches are level-triggered storage elements. They are simpler than flip-flops and work with the level (HIGH or LOW) of the control signal.
3. Clock Signal (Timing Element) :- A clock is a periodic signal used to synchronize all flip-flops in a sequential circuit.
4. Combinational Logic Circuit :- These are combination of logic gates (AND, OR, NOT, etc.) that process input data without memory.
5. Feedback Path A feedback loop connects outputs of flip-flops back to inputs of the combinational circuit.



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Types of Sequential Circuits

Synchronous Sequential Circuits: All memory elements are triggered by a common clock signal.

Examples: Counters, Shift Registers.

Asynchronous Sequential Circuits: Changes occur immediately when inputs change, without a clock.

Faster but more complex and prone to timing problems.

Memory Elements Used

1. Latches (Level-triggered): Latches are basic storage elements that operate with signal levels. Its input is governed by toggle switch (Level triggered) and Output changes as long as the enable (control) signal is active. ***Types: SR latch, D latch,***

2. Flip-Flops (Edge-triggered): Its input is governed by Clock signal (Edge triggered) Output changes only on clock edges (rising or falling).

Types: SR Flip-Flop, D Flip-Flop, JK Flip-Flop, T Flip-Flop

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Difference between Combinational and Sequential Circuits

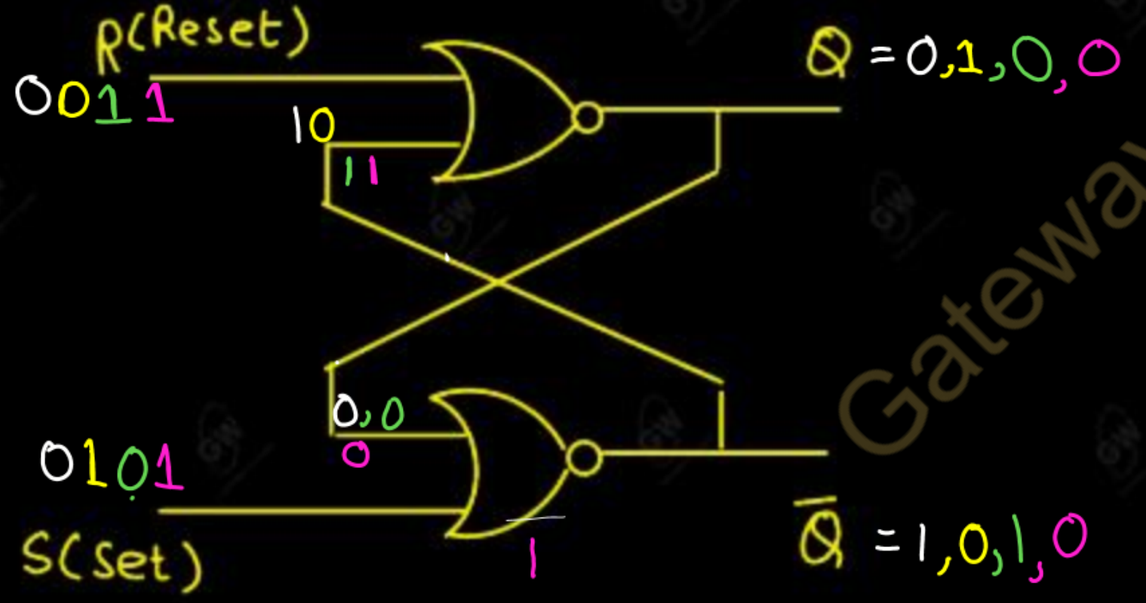
Feature	Sequential Circuits	Combinational Circuits
Definition	Output depends on current inputs and past states.	Output depends only on current inputs.
Memory	Contains memory elements (e.g., flip-flops, latches).	No memory elements; stateless.
Feedback	Uses feedback to store and utilize past states.	No feedback; outputs are purely input-driven.
Clock Dependency	Often synchronous, driven by a clock signal.	No clock required; operates instantaneously.
Complexity	More complex due to memory and state management.	Simpler, as it only processes current inputs.
Examples	Counters, registers, finite state machines.	Adders, multiplexers, encoders, decoders.
Timing	Outputs change at specific times (e.g., clock edges).	Outputs change immediately with input changes.
Applications	Used in systems requiring memory, timing, or sequencing (e.g., CPUs, memory units).	Used in arithmetic and logic operations (e.g., ALUs, logic gates).
State Dependency	State-dependent (state is stored and updated).	State-independent (no concept of state).

Gateway Classes

SR latch

SR Latch is also called as Set Reset Latch and implemented using two inputs: S (Set) and R (Reset). The S input sets the output to 1, while the R input resets the output to 0. When both S and R inputs are at 1, the latch is said to be in an "undefined" state.

Logic Diagram (Using NOR Gate)



Truth Table

	S	R	Q	Q̄	
(i)	0	0	0	1	→ No change
(ii)	1	0	1	0	→ Set
(iii)	0	1	0	1	→ Reset
(iv)	1	1	—	—	undefined state (Prohibited)

Race Cond^n

Gateway Classes

SR latch

Case-1 (When S= R=0)

$S=0$, $R=0$, $Q=0$, $\bar{Q}=1$

Then there is no change in state

Case-2 (When S= 0 , R=1)

$S=0$, $R=1$, $Q=0$, $\bar{Q}=1$

This it is a reset Condⁿ

Case-3 (When S=1, R=0)

$S=1$, $R=0$, $Q=1$, $\bar{Q}=0$

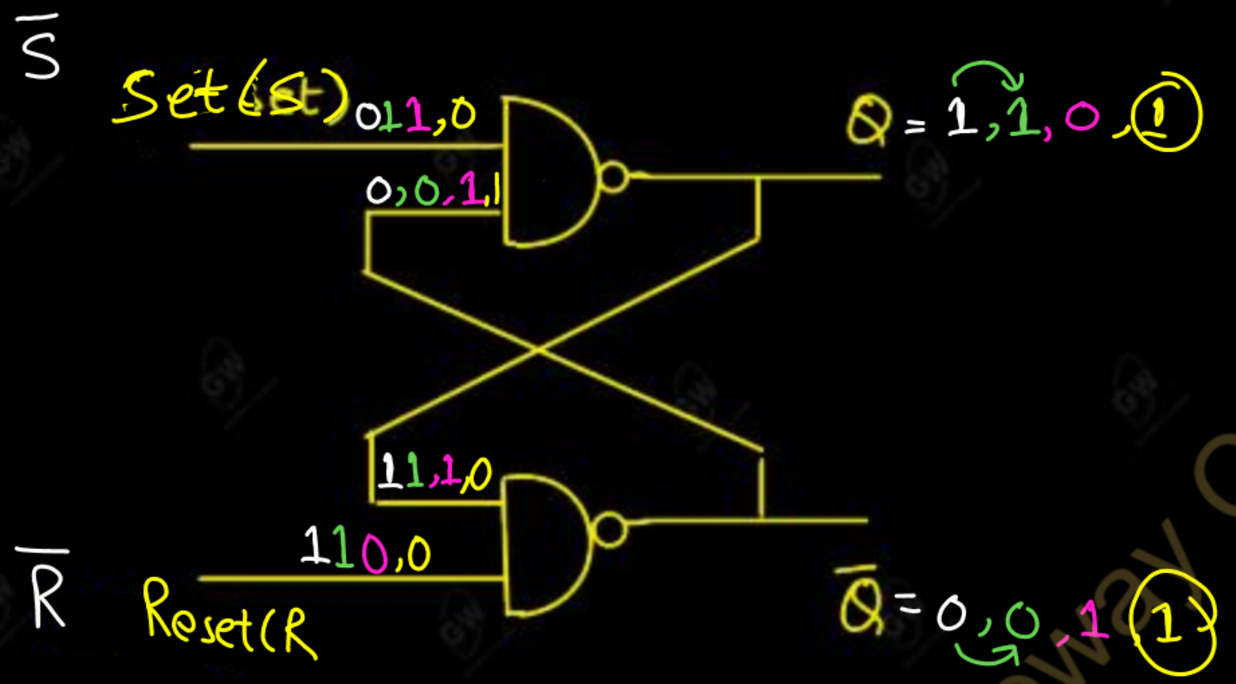
This is set condition

Case-4 (When S= 1, R=1)

$S=R=1$, Undefined state.

Gateway Classes

Logic Diagram (Using NAND Gate)



Truth Table

S	R	Q	$\bar{Q}$	
0	1	1	0	→ Set
1	1	1	0	→ No change
1	0	0	1	→ Reset
0	0	⟷	⟷	→ undefined (Race)

Gateway Classes

SR latch

Case-1 (When S= R=0)

S= 0
R=0

Q=
$\bar{Q}$= } undefined.

Case-2 (When S= 0 , R=1)

S=0
R=1

Q = 1
$\bar{Q}$ = 0 } set

Case-3 (When S=1, R=0)

S=1
R=0

Q = 0
$\bar{Q}$ = 1 } Reset

Case-4 (When S= 1, R=1)

S=1, R=1

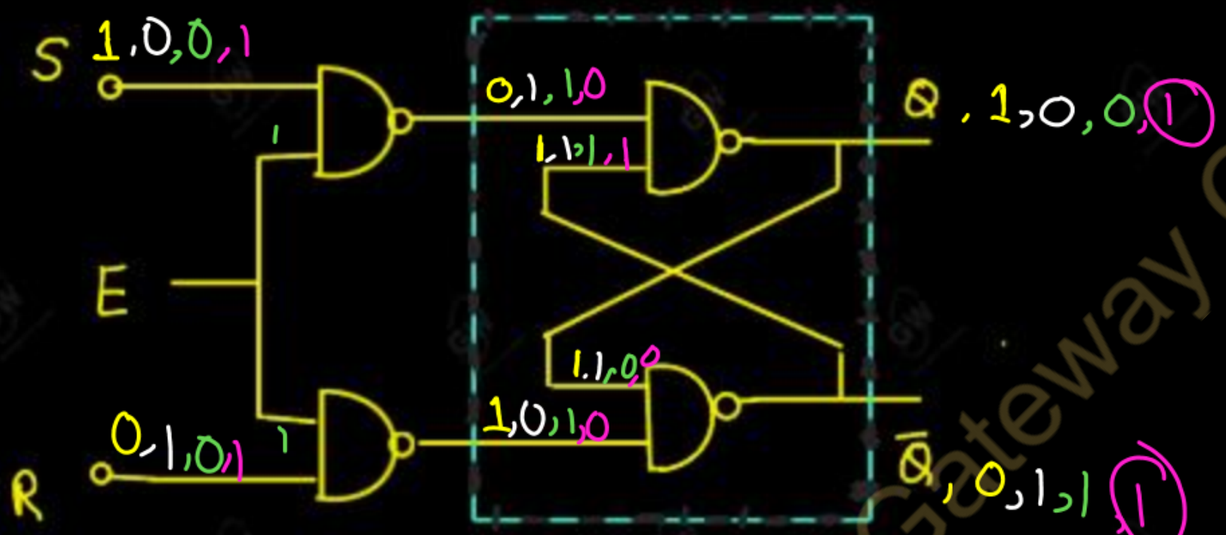
Q =1
$\bar{Q}$ =0 } No change

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Gated SR latch

A Gated SR latch is a SR latch with enable input which works when enable is 1 and retain the previous state when enable is 0.

Logic Diagram.



Truth Table

E	S	R	Q	$\bar{Q}$	
0	x	x	1	0	
1	1	0	1	0	→ Set
1	0	1	0	1	→ Reset
1	0	0	0	1	No change
1	1	1	⟷		undefined.

Gateway Classes

SR Gated latch Working

Case-1 (When S = x , R = x , E=0)

S=x , R=x , E=0 , $Q_{n+1} = Q_n$

$\overline{Q}_{n+1} = \overline{Q}_n$

Case-2 (When S= R=0 , E=1)

E=1 S=0 R=0 , Q = 0 , $\overline{Q}$ = 1 } No change

Case-3 (When S= 0 , R=1 , E=1)

E=1 S=0 R=1 Q = 0 , $\overline{Q}$ = 1 } Reset

Case-4 (When S=1, R=0 , E=1)

E= S=1 R=0 Q = 1 , $\overline{Q}$ = 0 } Set

Case-5 (When S= 1, R=1 , E=1)

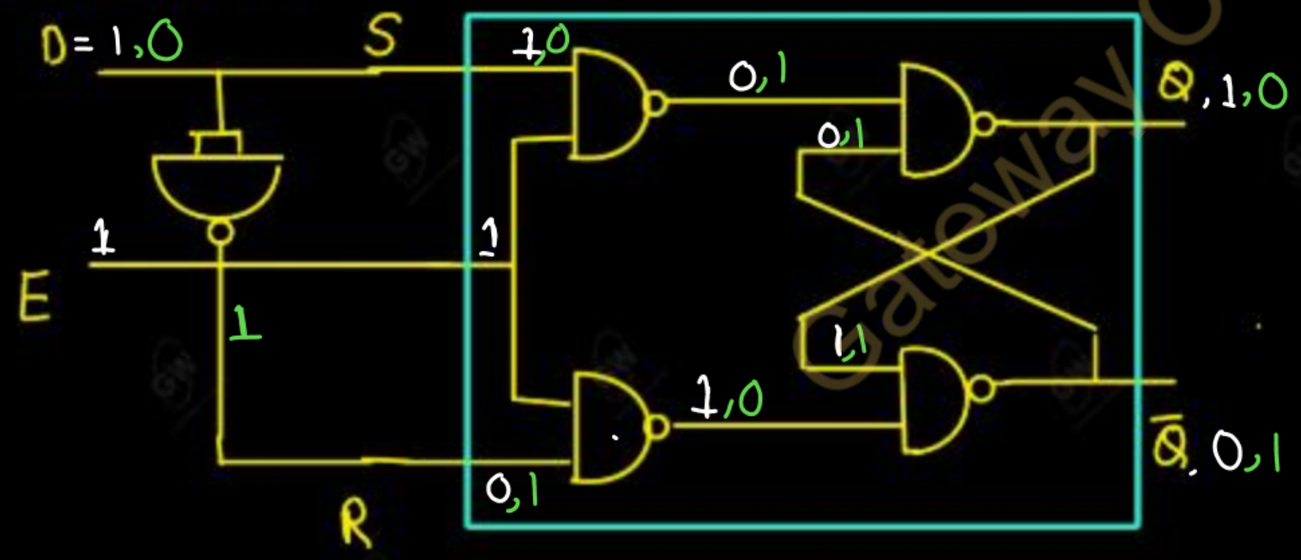
S=1=R=1 , Undefined

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D latch:- There is one drawback of SR Latch. That is the next state value can't be predicted when both the inputs S & R are one. So, you can overcome this difficulty by D Latch (Data Latch).

This circuit has single input D and two outputs Q(t) & Q(t)'. D Latch is obtained from SR Latch by placing an inverter between S amp;& R inputs and connect D input to S. That means the combinations, having same values, of S & R are eliminated.

Logic Diagram.



Truth Table

S.N.	E	D	Q_{n+1}	$\bar{Q}_{n+1}$	Comment
	0	x	1	0	—
	1	1	1	0	Set
	1	0	0	1	Reset

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D latch Working

Case-1 (D = 0 → S = 0 & R = 1)

D = 0 , S = 0, R = 1 } Q = 0, $\bar{Q}$ = 1 } Set

Case-2 (D = 1 → S = 1 & R = 0)

D = 1 , S = 1, R = 0 } Q = 1, $\bar{Q}$ = 0 } Reset

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Thank You

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