AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-3 Lec-1



Today's target

- Introduction to Sequential Circuits
- SR Latch ,D Latch
- PYQ

Avinash Sir

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

Sequential Circuits

Sequential circuits are a type of digital circuit where the output depends not only on the current inputs but also on the history of past inputs, which is stored as the circuit's state. They rely on feedback loops to retain information about previous states. They are widely used in systems requiring memory, timing, or sequential operations, such as counters, registers, and finite state machines.

Key Characteristics of Sequential Circuits:

- **Memory Elements:** Sequential circuits include memory components like flip-flops or latches, which store the state of the circuit.
- **Dependence on Past Inputs:** The output is a function of both current inputs and the stored state (past inputs).
- **Clock Signal:** Most sequential circuits are synchronous, meaning they operate in sync with a clock signal.

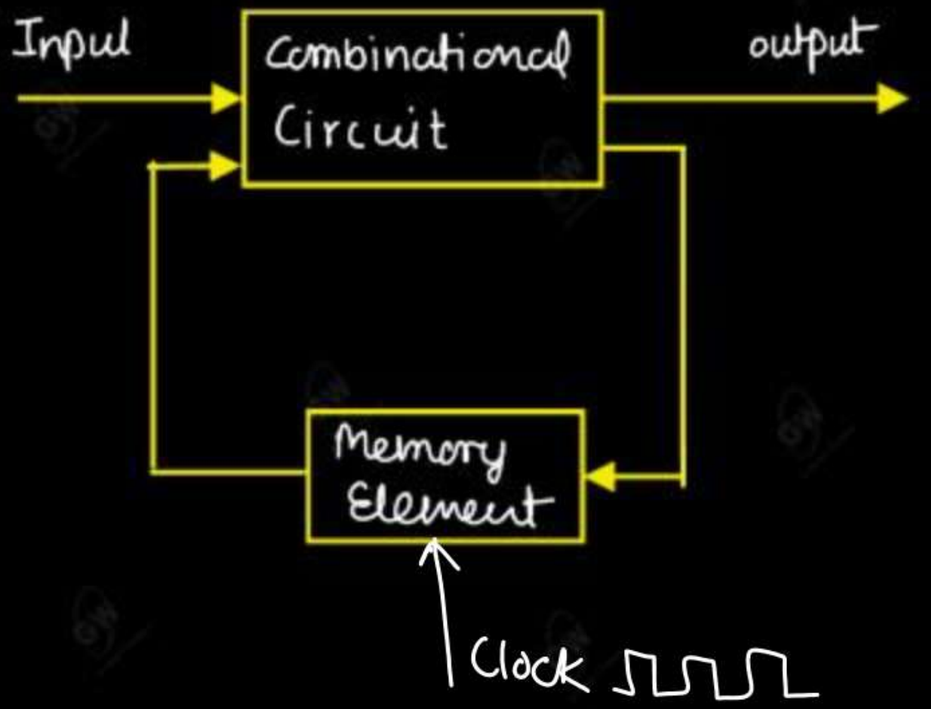
Gateway Classes

Basic Building Blocks of Sequential Circuits

AKTU -2023-24



1. Flip-Flops (Memory Elements): Flip-flops are the fundamental memory units in sequential circuits. They store 1 bit of data (0 or 1). SR, JK, D, T
2. Latches :-Latches are level-triggered storage elements. They are simpler than flip-flops and work with the level (HIGH or LOW) of the control signal.
3. Clock Signal (Timing Element) :- A clock is a periodic signal used to synchronize all flip-flops in a sequential circuit.
4. Combinational Logic Circuit :- These are combination of logic gates (AND, OR, NOT, etc.) that process input data without memory.
5. Feedback Path A feedback loop connects outputs of flip-flops back to inputs of the combinational circuit.



Gateway Classes

Types of Sequential Circuits

Synchronous Sequential Circuits: All memory elements are triggered by a common clock signal.

Examples: Counters, Shift Registers.

Asynchronous Sequential Circuits: Changes occur immediately when inputs change, without a clock.

Faster but more complex and prone to timing problems.

Memory Elements Used

1. Latches (Level-triggered): Latches are basic storage elements that operate with signal levels. Its input is governed by toggle switch (Level triggered) and Output changes as long as the enable (control) signal is active. ***Types: SR latch, D latch,***

2. Flip-Flops (Edge-triggered): Its input is governed by Clock signal (Edge triggered) Output changes only on clock edges (rising or falling).

Types: SR Flip-Flop, D Flip-Flop, JK Flip-Flop, T Flip-Flop

Gateway Classes

Difference between Combinational and Sequential Circuits

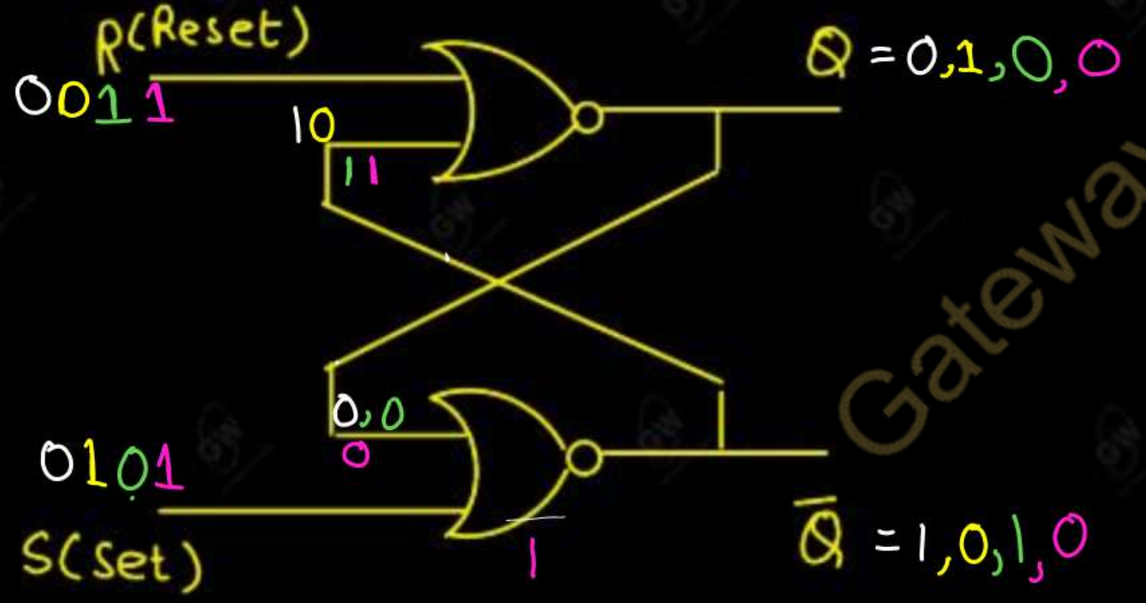
Feature	Sequential Circuits	Combinational Circuits
Definition	Output depends on current inputs and past states.	Output depends only on current inputs.
Memory	Contains memory elements (e.g., flip-flops, latches).	No memory elements; stateless.
Feedback	Uses feedback to store and utilize past states.	No feedback; outputs are purely input-driven.
Clock Dependency	Often synchronous, driven by a clock signal.	No clock required; operates instantaneously.
Complexity	More complex due to memory and state management.	Simpler, as it only processes current inputs.
Examples	Counters, registers, finite state machines.	Adders, multiplexers, encoders, decoders.
Timing	Outputs change at specific times (e.g., clock edges).	Outputs change immediately with input changes.
Applications	Used in systems requiring memory, timing, or sequencing (e.g., CPUs, memory units).	Used in arithmetic and logic operations (e.g., ALUs, logic gates).
State Dependency	State-dependent (state is stored and updated).	State-independent (no concept of state).

Gateway Classes

SR latch

SR Latch is also called as Set Reset Latch and implemented using two inputs: S (Set) and R (Reset). The S input sets the output to 1, while the R input resets the output to 0. When both S and R inputs are at 1, the latch is said to be in an "undefined" state.

Logic Diagram (Using NOR Gate)



Truth Table

	S	R	Q	$\bar{Q}$	
(i)	0	0	0	1	→ No change
(ii)	1	0	1	0	→ Set
(iii)	0	1	0	1	→ Reset
(iv)	1	1	—	—	undefined state (Prohibited)

Race Cond^{n}

Gateway Classes

SR latch

Case-1 (When S= R=0)

$S=0$, $R=0$, $Q=0$, $\bar{Q}=1$

Then there is no change in state

Case-2 (When S= 0 , R=1)

$S=0$, $R=1$, $Q=0$, $\bar{Q}=1$

This it is a reset Cond^n

Case-3 (When S=1, R=0)

$S=1$, $R=0$, $Q=1$, $\bar{Q}=0$

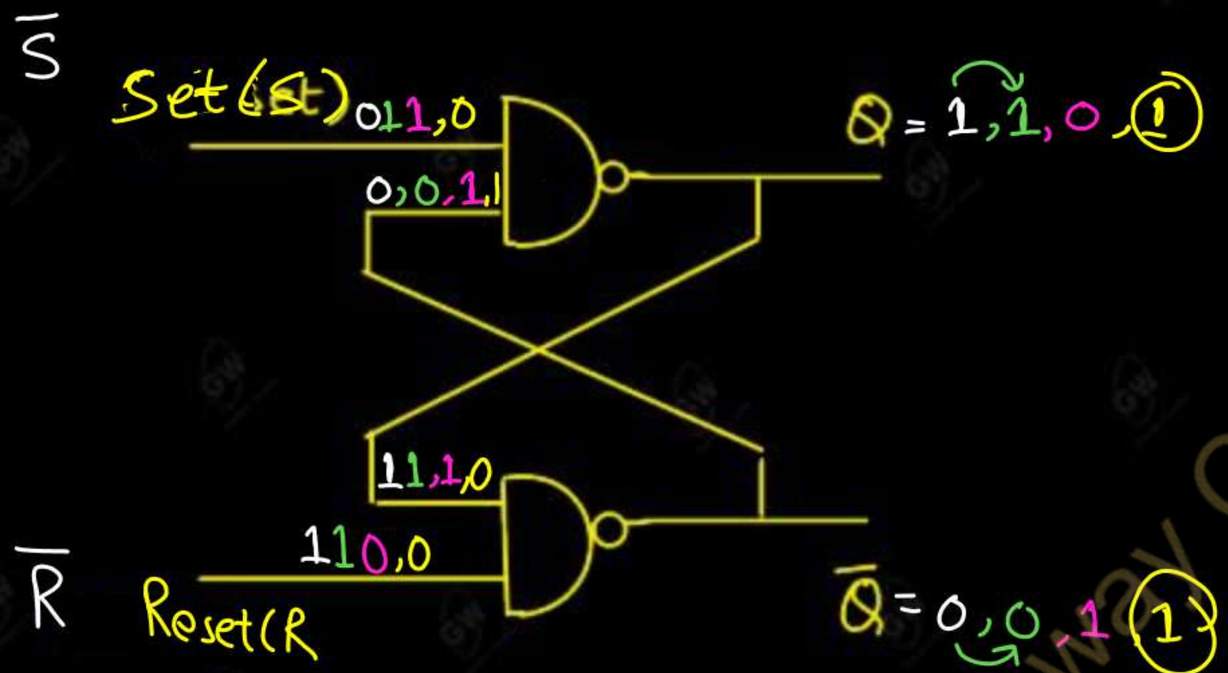
This is set condition

Case-4 (When S= 1, R=1)

$S=R=1$, Undefined state.

Gateway Classes

Logic Diagram (Using NAND Gate)



Truth Table

S	R	Q	$\bar{Q}$	
0	1	1	0	→ Set
1	1	1	0	→ No change
1	0	0	1	→ Reset
0	0	⟷	⟷	→ undefined (Race)

Gateway Classes

SR latch

Case-1 (When S= R=0)

S= 0
R=0

Q =
$\bar{Q}$ = } undefined.

Case-2 (When S= 0 , R=1)

S=0
R=1

Q = 1
$\bar{Q}$ = 0 } set

Case-3 (When S=1, R=0)

S=1
R=0

Q = 0
$\bar{Q}$ = 1 } Reset

Case-4 (When S= 1, R=1)

S=1, R=1

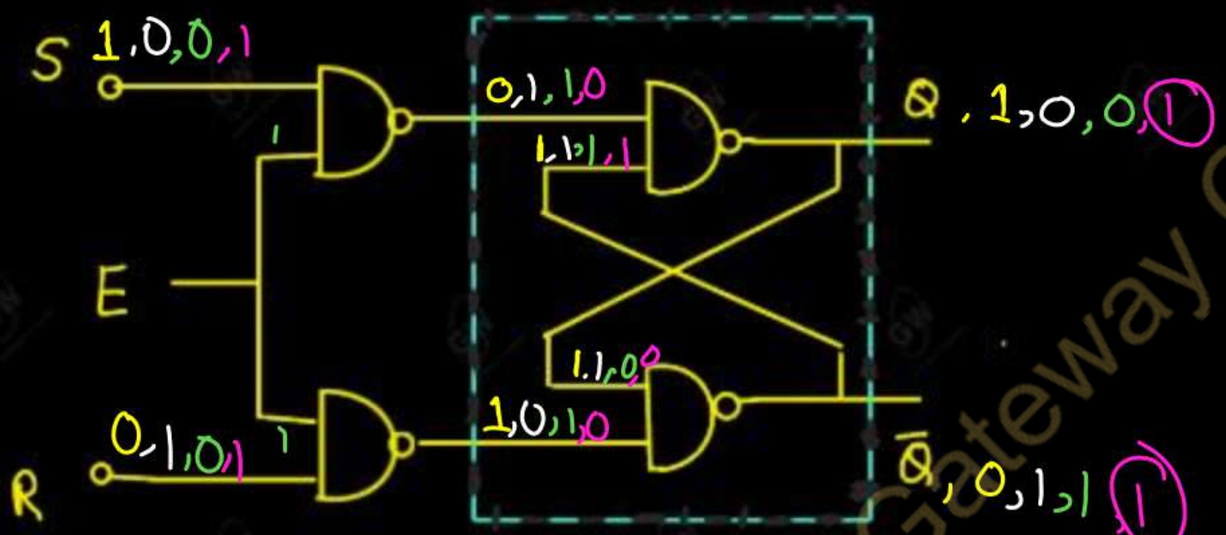
Q =1
$\bar{Q}$ =0 } No change

Gateway Classes

Gated SR latch

A Gated SR latch is a SR latch with enable input which works when enable is 1 and retain the previous state when enable is 0.

Logic Diagram.



Truth Table

E	S	R	Q	$\bar{Q}$	
0	x	x	1	0	
1	1	0	1	0	→ Set
1	0	1	0	1	→ Reset
1	0	0	0	1	No change
1	1	1	⟷		undefined.

Gateway Classes

SR Gated latch Working

Case-1 (When S = x , R = x , E=0)

S=x , R=x , E=0 , $Q_{n+1} = Q_n$

$\overline{Q}_{n+1} = \overline{Q}_n$

Case-2 (When S= R=0 , E=1)

E=1 S=0 R=0 , Q = 0 , $\overline{Q}$ = 1 } No change

Case-3 (When S= 0 , R=1 , E=1)

E=1 S=0 R=1 Q = 0 , $\overline{Q}$ = 1 } Reset

Case-4 (When S=1, R=0 , E=1)

E= S=1 R=0 Q = 1 , $\overline{Q}$ = 0 } Set

Case-5 (When S= 1, R=1 , E=1)

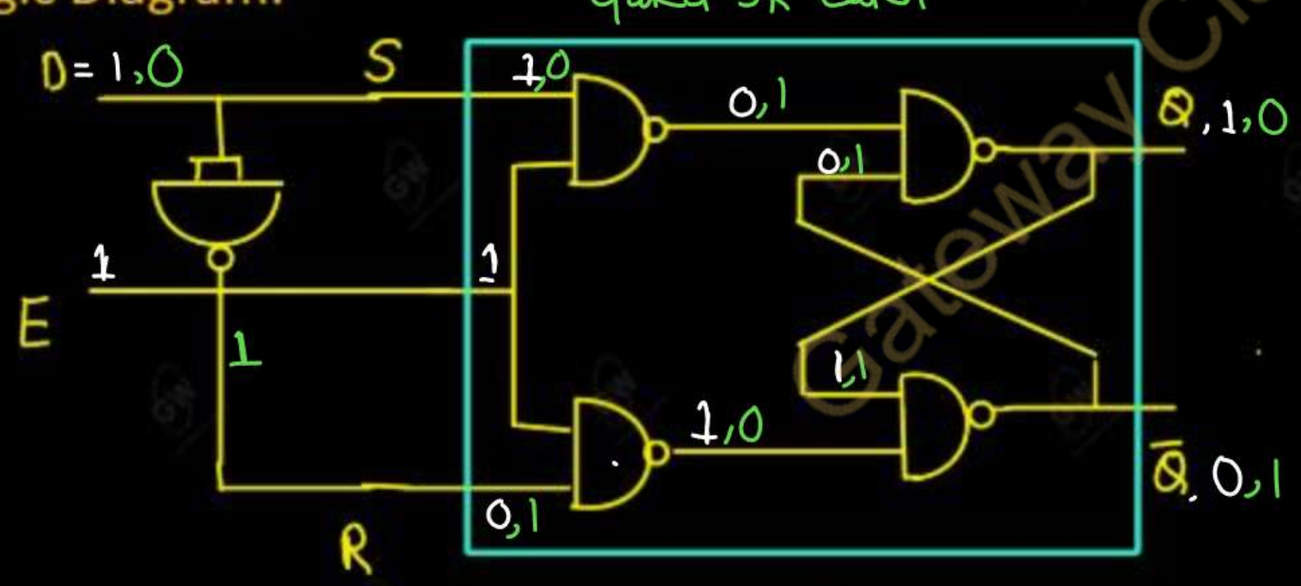
S=1=R=1 , Undefined

Gateway Classes

D latch:- There is one drawback of SR Latch. That is the next state value can't be predicted when both the inputs S & R are one. So, you can overcome this difficulty by D Latch (Data Latch).

This circuit has single input D and two outputs Q(t) & Q(t)'. D Latch is obtained from SR Latch by placing an inverter between S amp;& R inputs and connect D input to S. That means the combinations, having same values, of S & R are eliminated.

Logic Diagram.



Truth Table

S.N.	E	D	Q_{n+1}	$\bar{Q}_{n+1}$	Comment
	0	x	1	0	—
	1	1	1	0	Set
	1	0	0	1	Reset

Gateway Classes

D latch Working

Case-1 (D = 0 → S = 0 & R = 1)

D = 0 , S = 0, R = 1 } Q = 0, $\bar{Q}$ = 1 } Set

Case-2 (D = 1 → S = 1 & R = 0)

D = 1 , S = 1, R = 0 } Q = 1, $\bar{Q}$ = 0 } Reset

Gateway Classes

AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-3 Lec-2



Avinash Sir

Today's target

- Types of Flip Flop
- Extinction Table
- PYQ

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

Flip Flops:-

The flip-flop is a circuit that maintains a state until directed by input to change the state. A basic flip-flop can be constructed using four-NAND or four-NOR gates.

A flip-flop is popularly known as the basic digital memory circuit. It has its two states as logic 1(High) and logic 0 (Low) states.

Types of Flip-Flops

- SR Flip Flop
- JK Flip Flop
- D Flip Flop
- T Flip Flop

Gateway Classes

Differences between latches and flip-flops

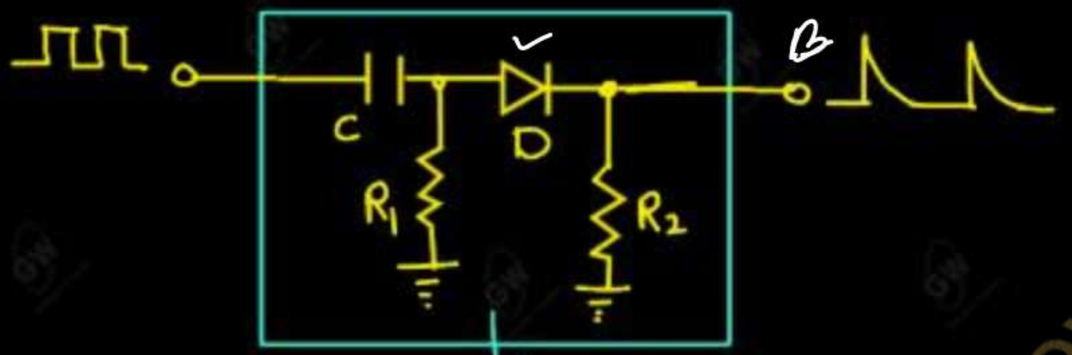
Latches	Flip-flops
Level triggered	Edge triggered
Asynchronous device	Synchronous device
Doesn’t contain clock signal	Contains a clock signal
It will change its state as long as it is enabled	It will change its state only during a given clock cycle
Consumes less power	Consumes more power
Faster	Slower
Examples: D-Latch, T-Latch	Examples: D-Flip flop, T-Flop flop

Gateway Classes

Edge Triggered Flip Flops

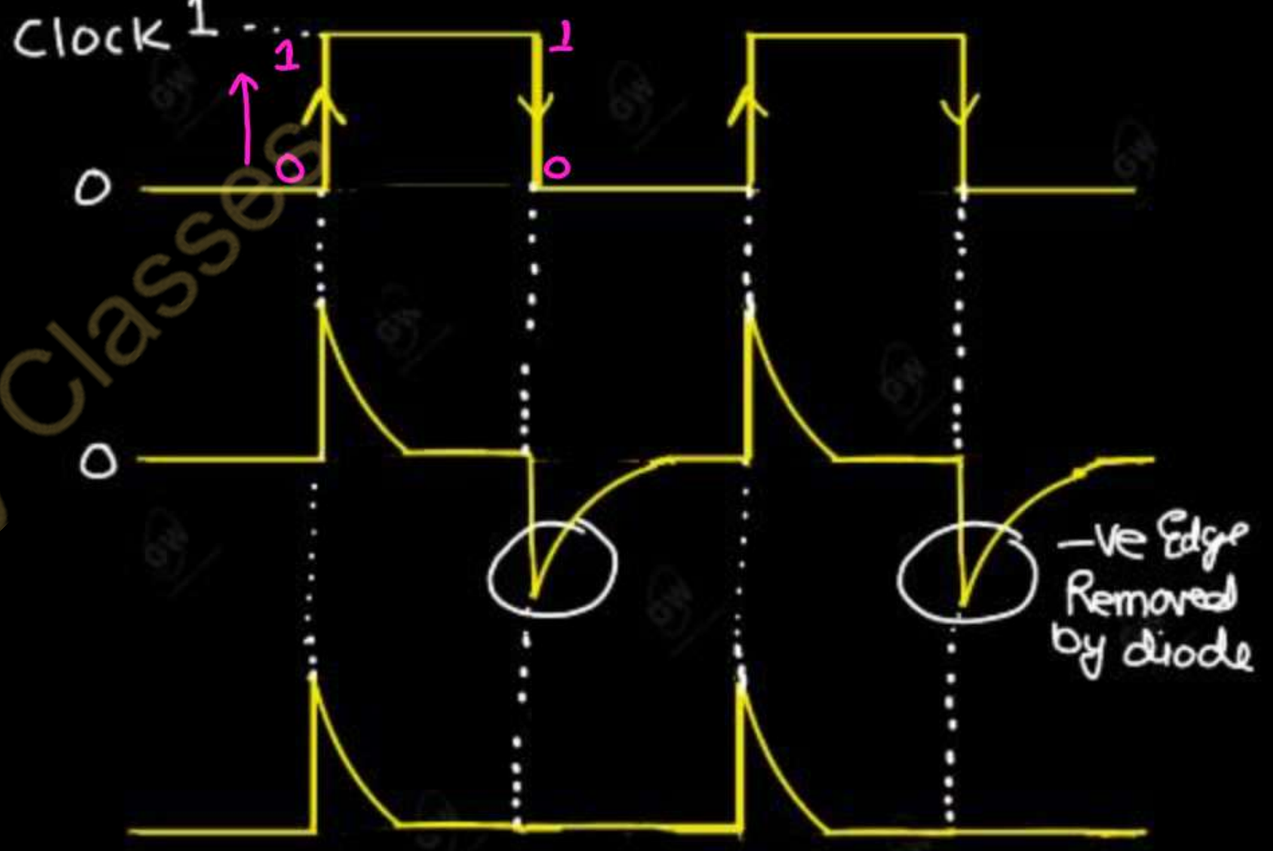
0 → 1 → +ve edge, rising.
1 → 0 → -ve edge, falling

- The input of flip flop is governed by flip flop in two ways .
  - (i) Positive Edge Triggered Flip Flop
  - (i) Negative Edge Triggered Flip Flop



↳ Differentiator

Clock Edge triggered Circuit



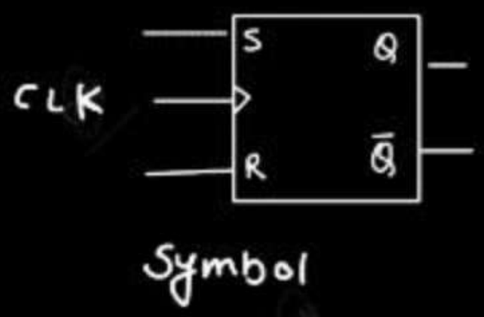
Positive Edge triggered pulse.

Gateway Classes

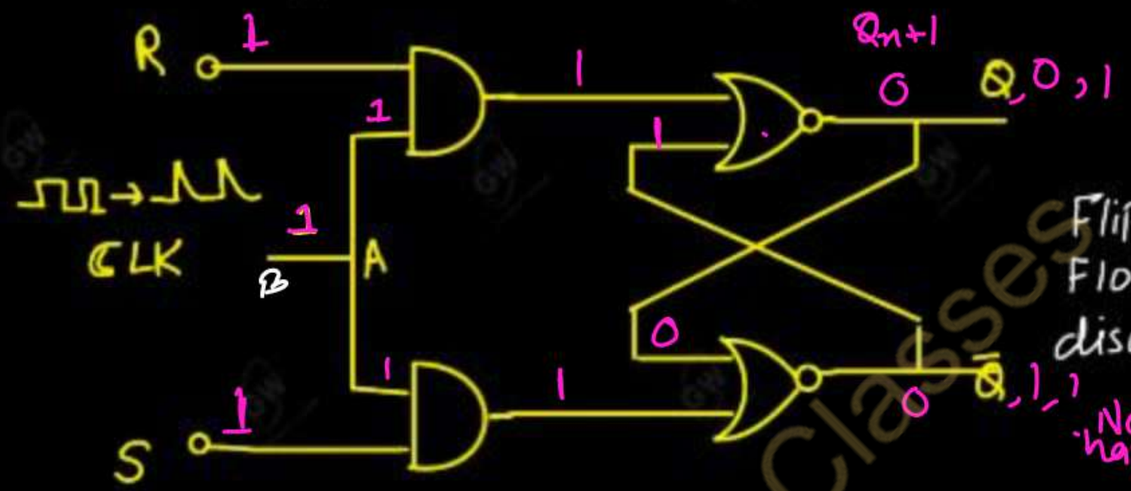
Positive edge Triggered SR Flip Flops

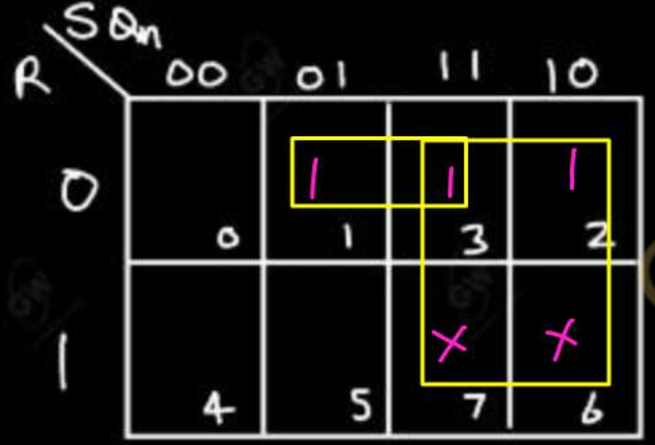
AKTU -2024-25

- SR flip-flop operates with only positive clock transitions.



Symbol





$Q_{n+1} = S + \bar{R}Q_n$

Characteristic Equation

CLK	R	S	Q_n Present State Q_n	Q_{n+1} Next State (Q_{n+1})
0	x	x	Q_n	Q_n
⌋	x	x	Q_n	Q_n
↓	x	x	Q_n	Q_n
↑	0	0	0	0
↑	0	0	1	1
↑	0	1	0	1
↑	0	1	1	1
↑	1	0	0	0
↑	1	0	1	0
↑	1	1	0	x
↑	1	1	1	x

Flip Flop disabled

No change

Set

Flip flop Enabled for +ve Edge

Reset

invalid

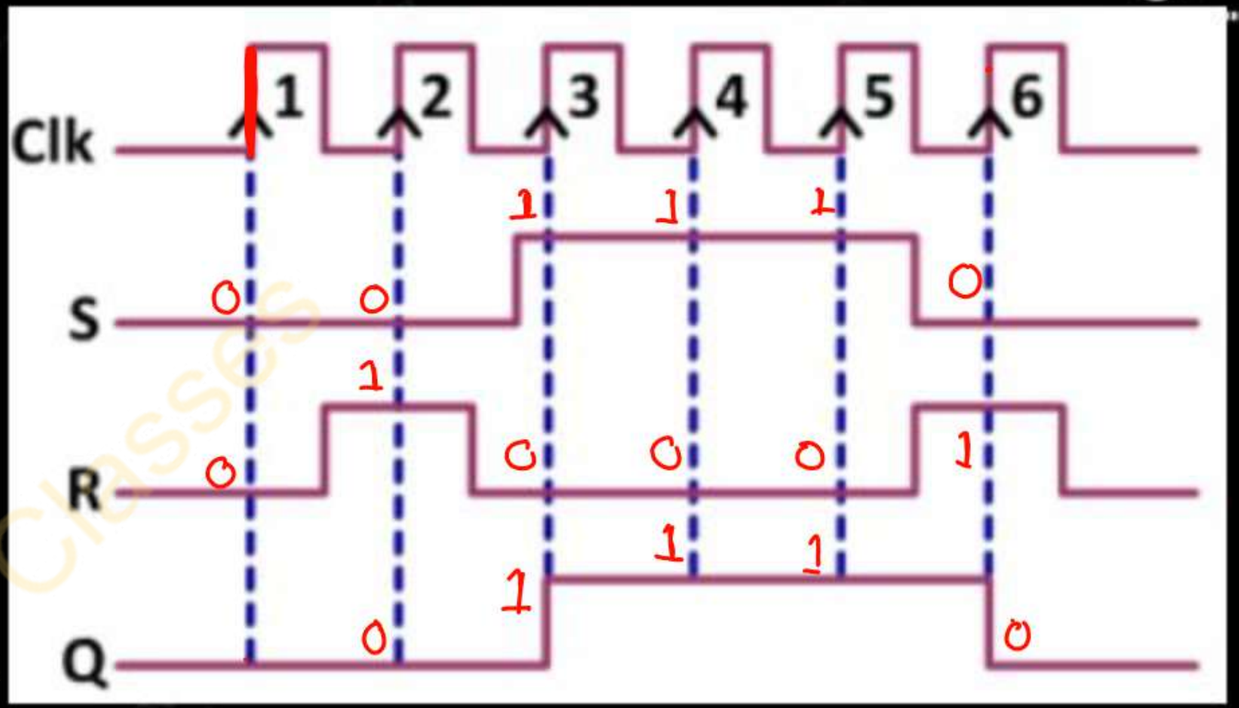
Gateway Classes

Wave Form

The output waveform is shown and is explained as follows

1. During the 1st positive clock edge, S=R=0 so Q =0
2. During 2nd positive clock edge, S=0 and R=1, Q =0 .
3. During 3rd positive clock edge, S=1 and R=0, Q=1.
4. During 4th positive clock edge, S=1 and R=0, Q=1

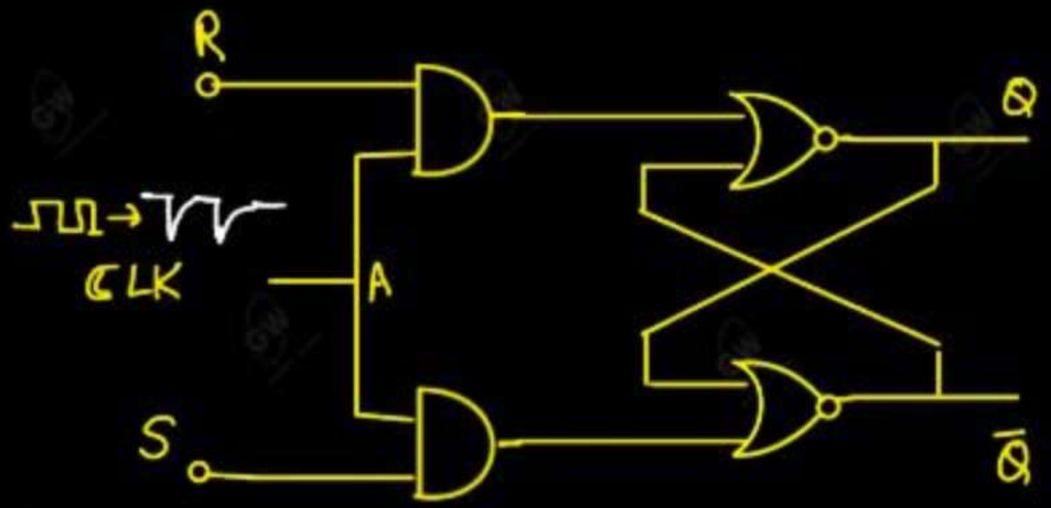
   Output is same at 5th clock pulse also .
5. During 6th positive clock edge, S=0 and R=1, Q=0

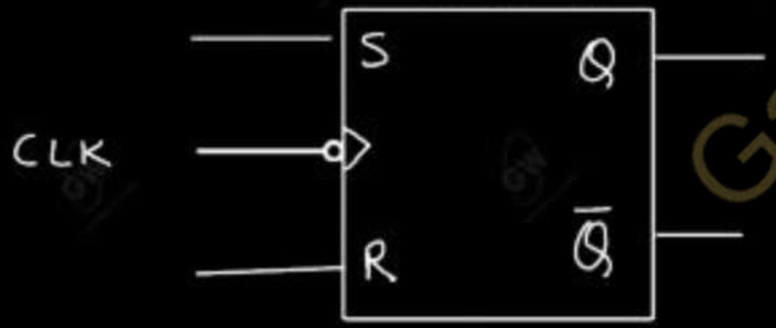


Gateway Classes

Negative edge Triggered SR Flip Flops

SR flip-flop operates with only negative clock transitions.





			Q_n	Q_{n+1}
CLK	R'	S'	Present State Q_n	Next State (Q_{n+1})
0	x	x	Q_n	Q_n
1	x	x	Q_n	Q_n
↑	x	x	Q_n	Q_n
↓	0	0	0	0
↓	0	0	1	1
↓	0	1	0	1
↓	0	1	1	1
↓	1	0	0	0
↓	1	0	1	0
↓	1	1	0	x
↓	1	1	1	x

Flip Flop disabled

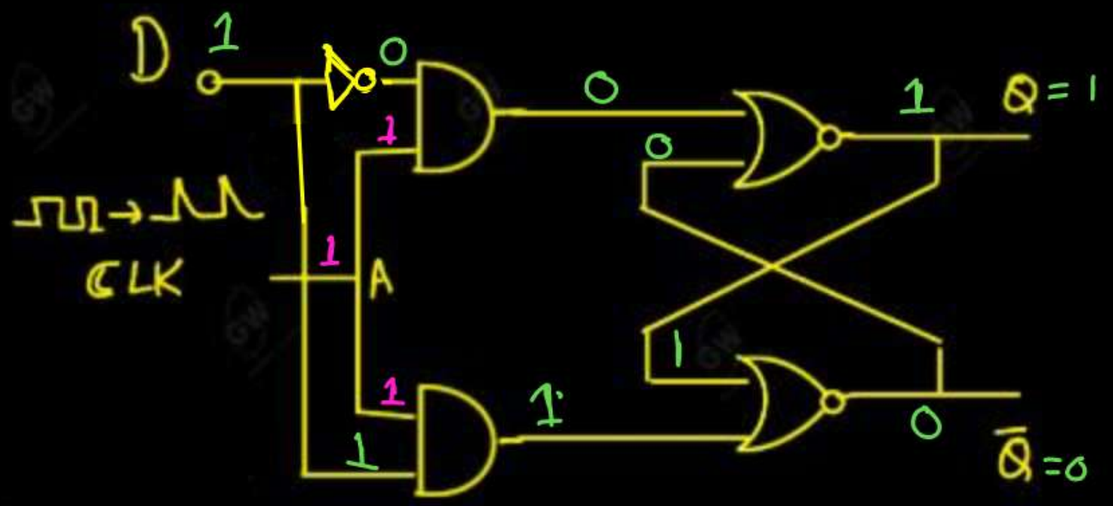
Flip flop Enabled for +ve Edge

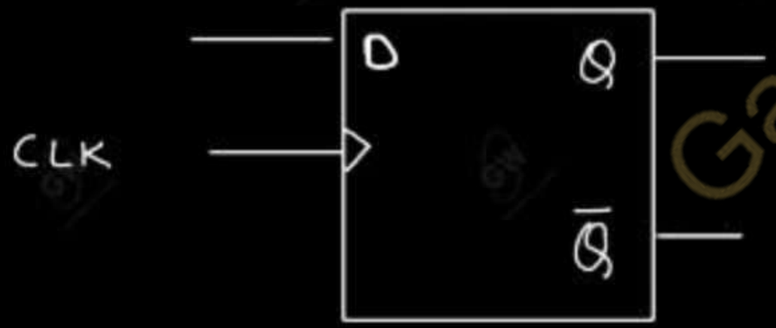
Gateway Classes

Positive edge Triggered D Flip Flops

AKTU -2024-25, 2023-24,2022-23

flip-flop operates with only positive clock transitions.

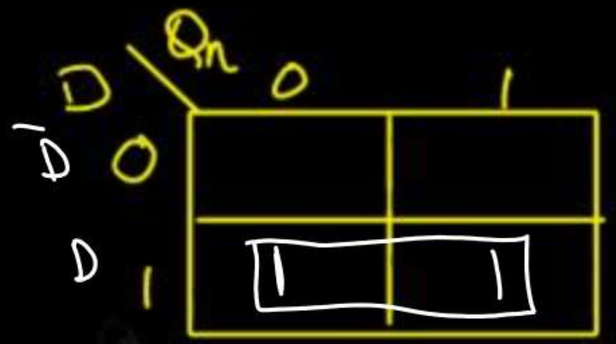




CLK	D	Present state Q_n	Next State (Q_{n+1})
0	x	Q_n	Q_n
⌋	x	Q_n	Q_n
↓	x	Q_n	Q_n
↑	0	0	0
↑	0	1	0
↑	1	0	1
↑	1	1	1

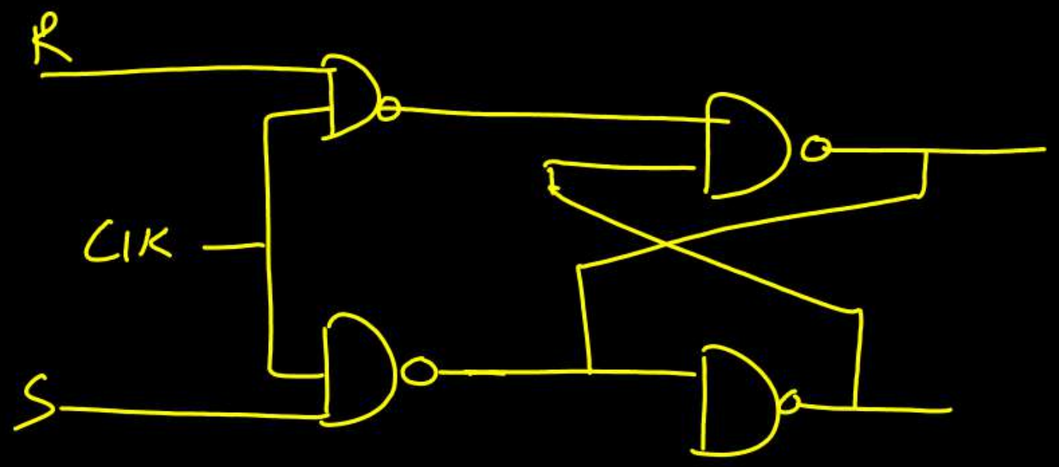
Flip Flop disabled

Flip flop Enabled for +ve Edge



$Q_{n+1} = D$

Gateway Classes



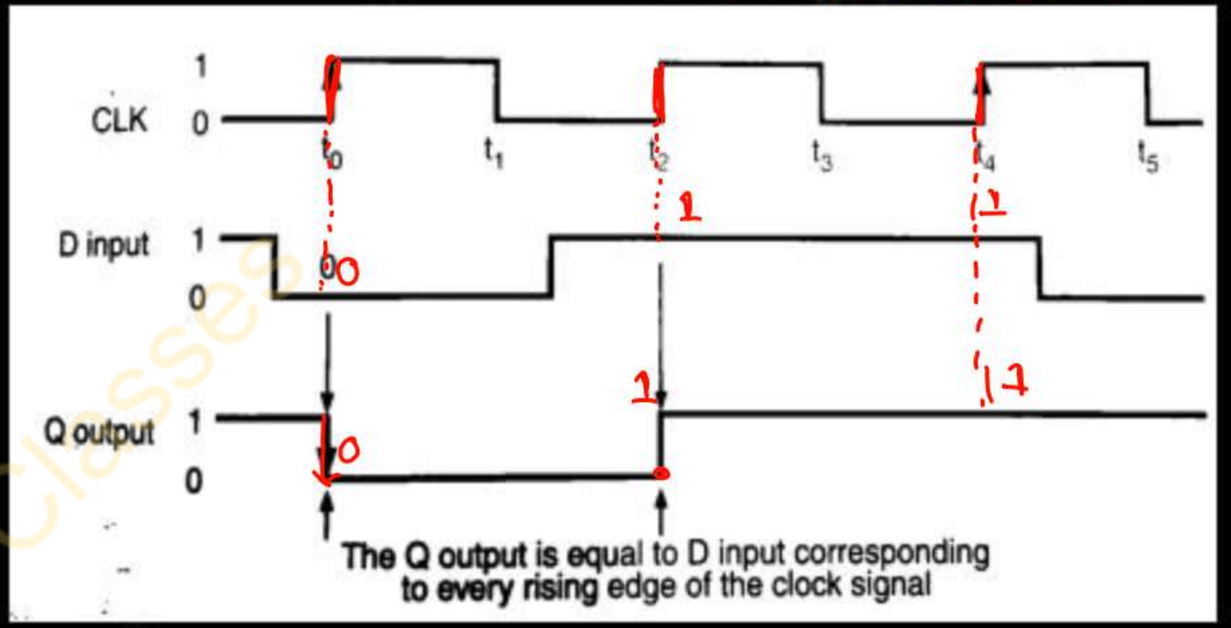
Gateway Classes

Positive edge Triggered D Flip Flop Waveform

AKTU -2024-25, 2023-24,2022-23

The output waveform is shown and is explained as follows

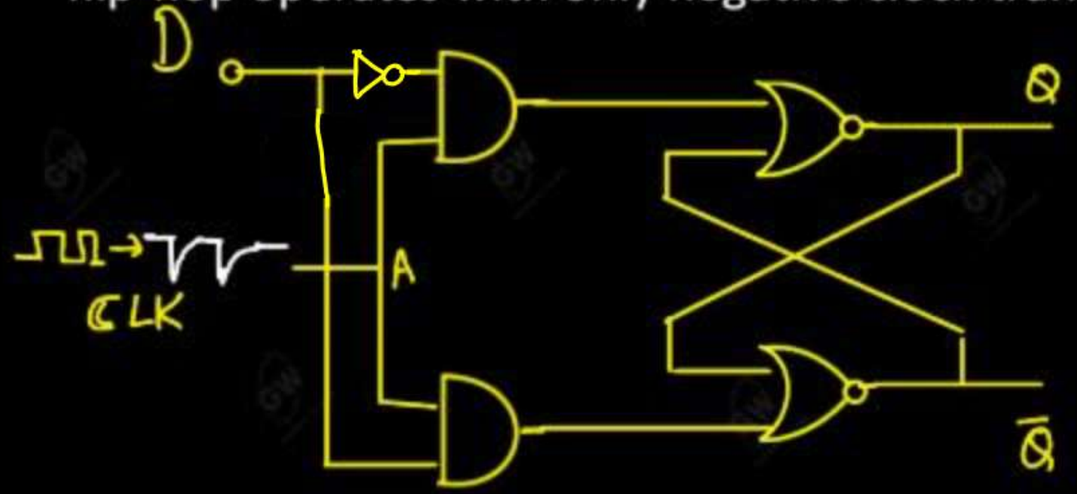
1. 1st Positive clock edge, D=0 so the output which is initially high will now change to logic 0.
2. 2nd Positive clock edge, D=1 so the output goes high.
3. 3rd Positive clock edge, D=1 so the output is still high.
4. 4th Positive clock edge, D=1 so the output goes high.

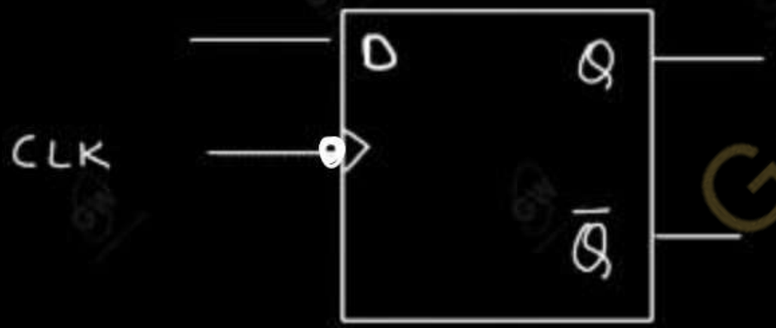


Gateway Classes

Negative edge Triggered D Flip Flops

flip-flop operates with only negative clock transitions.





CLK	D	Q_n Present State Q_n	Q_{n+1} Next State (Q_{n+1})
0	x	Q_n	Q_n
1	x	Q_n	Q_n
↑	x	Q_n	Q_n
↓	0	0	0
↓	0	1	0
↓	1	0	1
↓	1	1	1

Flip Flop disabled

Flip flop Enabled for −ve Edge

CLK	D	Q_n	Q_{n+1}
⎍	0	0	0
⎍	0	1	0
⎍	1	0	1
⎍	1	1	1

Gateway Classes

Negative edge Triggered D Flip Flop Waveform

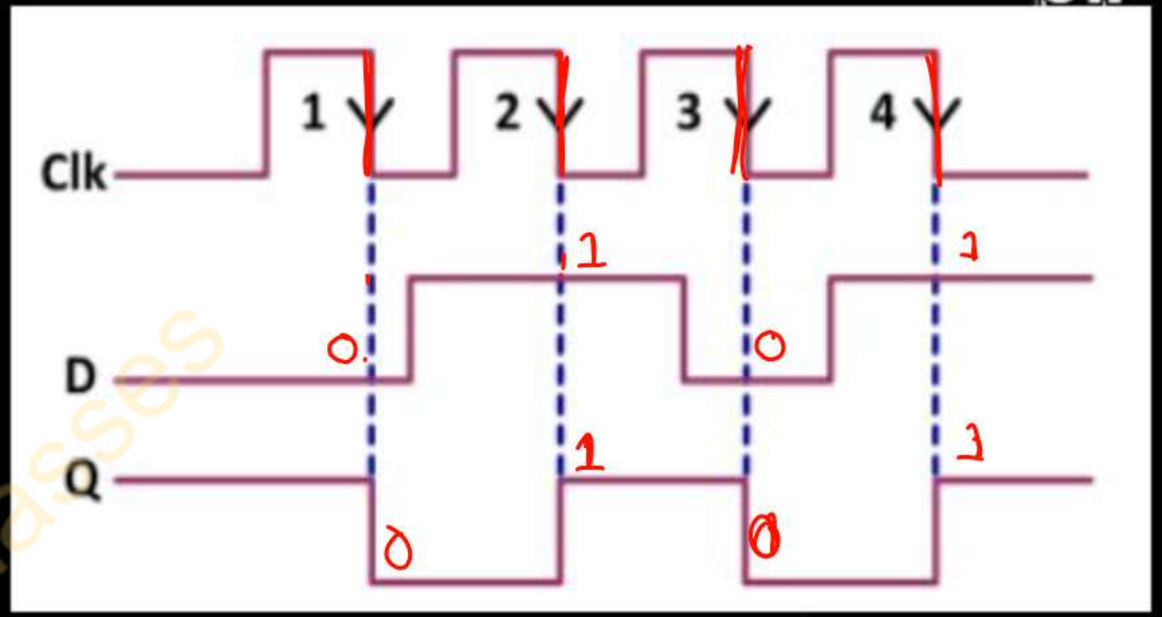
The output waveform is shown and is explained as follows

1. 1st negative clock edge, D=0 so the output which is initially SET will now change to logic 0.

2. 2nd negative clock edge, D=1 so the output goes high.

3. 3rd negative clock edge, D=0 so the output goes low.

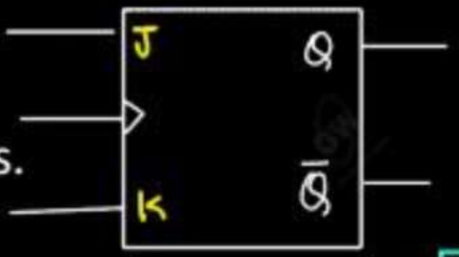
4. 4th negative clock edge, D=1 so the output goes high.



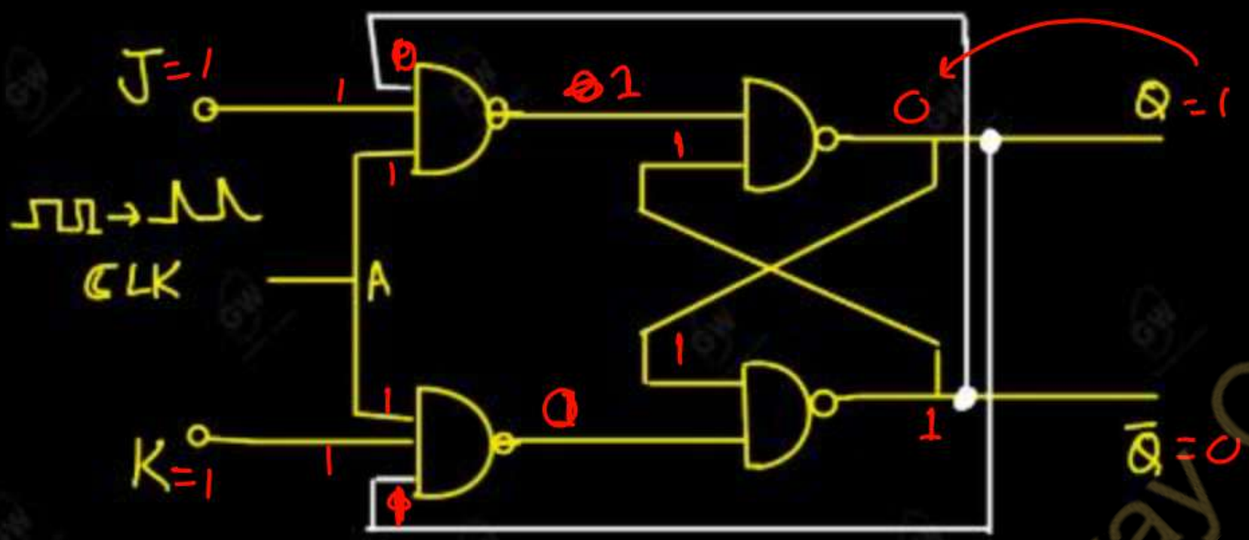
Gateway Classes

Positive edge Triggered JK Flip Flops

- JK flip-flop operates with only positive clock transitions.



AKTU -2024-25



CLK	J	K	Q_n Present State Q_n	Q_{n+1} Next State (Q_{n+1})
0	x	x	Q_n	Q_n
⌋	x	x	Q_n	Q_n
↓	x	x	Q_n	Q_n
↑	0	0	0	0
↑	0	0	1	1
↑	0	1	0	0
↑	0	1	1	0
↑	1	0	0	1
↑	1	0	1	1
↑	1	1	0	1
↑	1	1	1	0

Flip Flop disabled

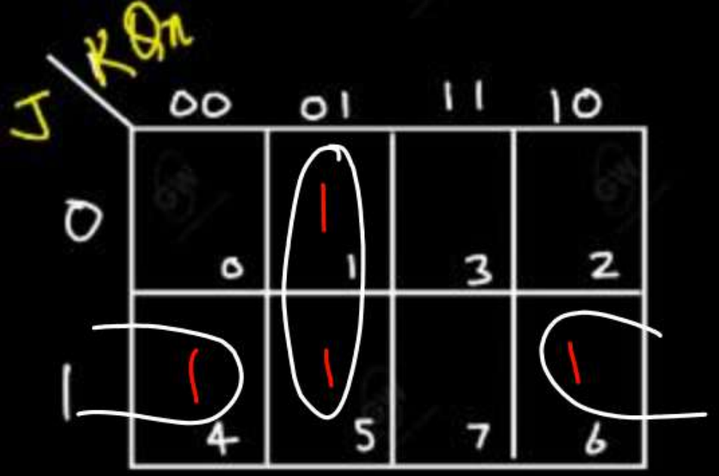
No change

Reset

Flip flop Enabled for +ve Edge

Set

Toggle

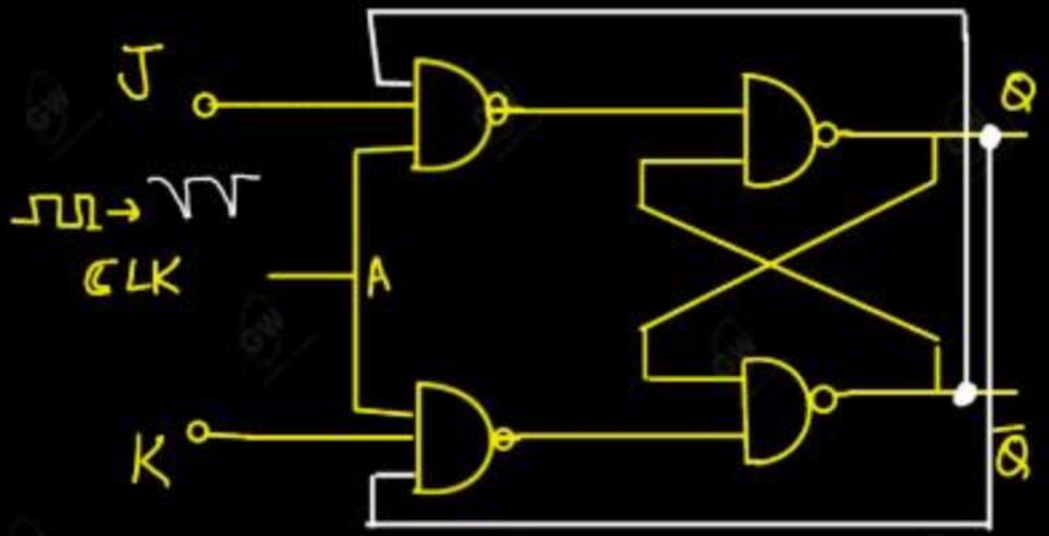


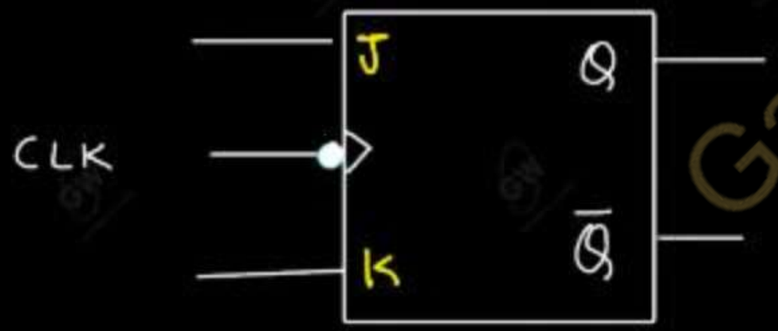
$$Q_{n+1} = \bar{K}Q_n + J\bar{Q}_n$$

Gateway Classes

Negative edge Triggered JK Flip Flops

JK flip-flop operates with only negative clock transitions.





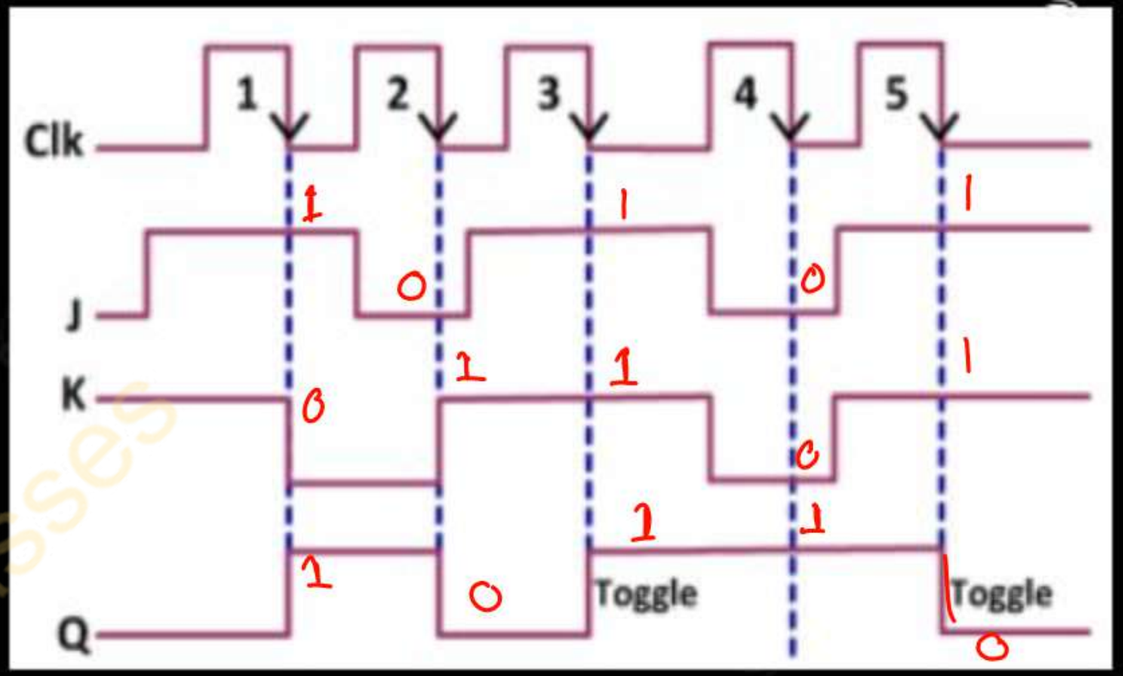
			Q_n	Q_{n+1}
CLK	J	K	Present State Q_n	Next State (Q_{n+1})
0	x	x	Q_n	Q_n
1	x	x	Q_n	Q_n
↑	x	x	Q_n	Q_n
↓	0	0	0	0
↓	0	0	1	1
↓	0	1	0	0
↓	0	1	1	0
↓	1	0	0	1
↓	1	0	1	1
↓	1	1	0	1
↓	1	1	1	0

Flip Flop disabled

Flip flop Enabled for +ve Edge

Gateway Classes

Negative edge Triggered JK Flip Flop waveform



The output waveform is shown and is explained as follows

1. 1st negative clock edge, J=1 and K=0 so the output which is initially RESET will now change to logic 1.

2. 2nd negative clock edge, J=0 and K=1 so the output goes low.

3. 3rd negative clock edge, J=K=1 so the output toggles i.e. initially it was in low state now the output goes high.

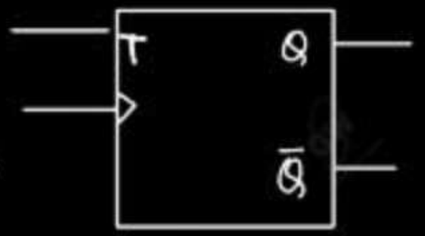
4. 4th negative clock edge, J=K=0 so the output retains its last value which is a high state.

5. 5th negative clock edge, J=K=1, the output will toggle, the last state was high so at 5th negative clock edge the output goes low.

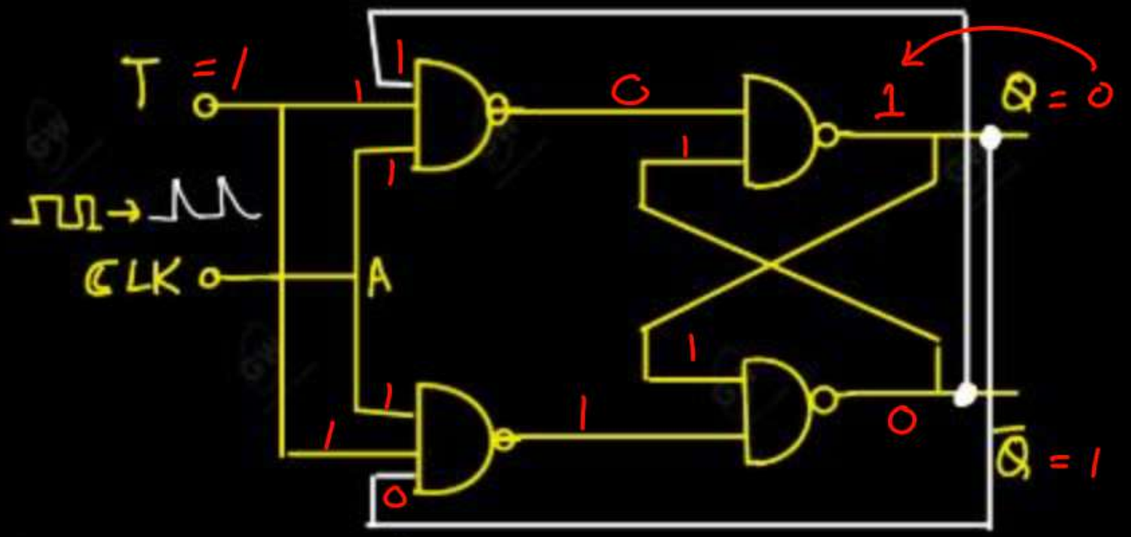
Gateway Classes

Positive edge Triggered T Flip Flops

- T flip-flop operates with only positive clock transitions.



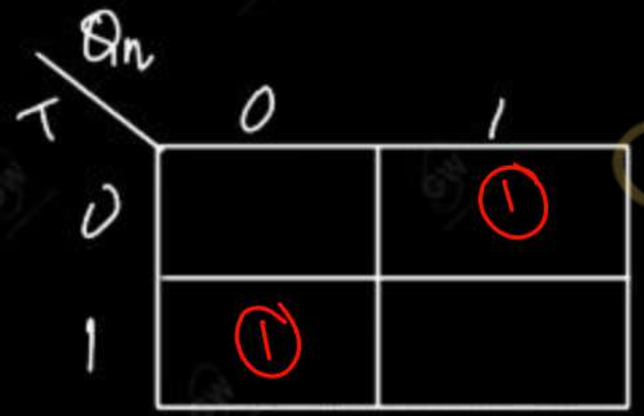
AKTU -2023-24



CLK	T	Q_n Present State Q_n	Q_{n+1} Next State (Q_{n+1})
0	x	Q_n	Q_n
⌋	x	Q_n	Q_n
↓	x	Q_n	Q_n
↑	0	0	0
↑	0	1	1
↑	1 ✓	0	1
↑	1 ✓	1	0

Flip Flop disabled

No change ← Flip flop Enabled for +ve Edge

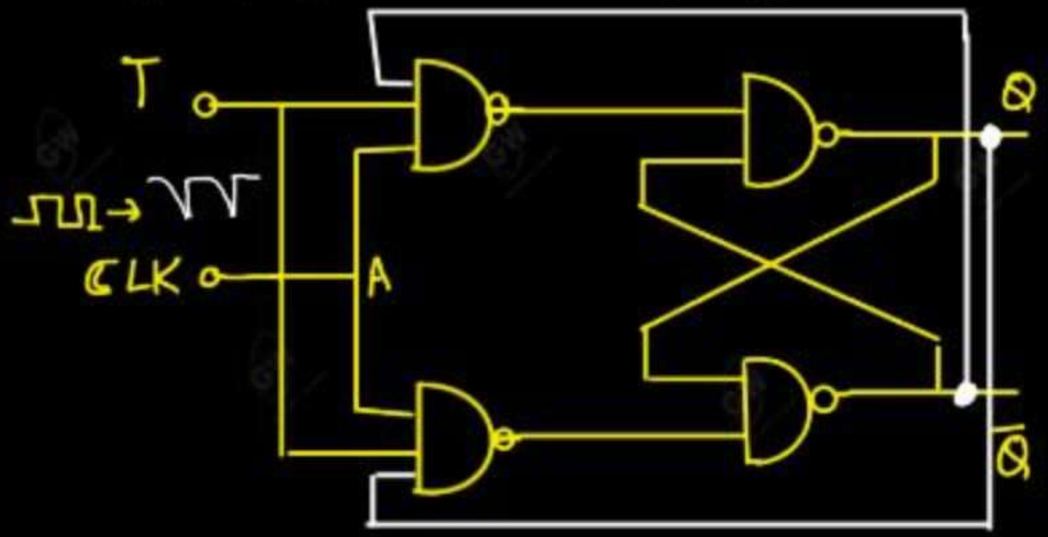


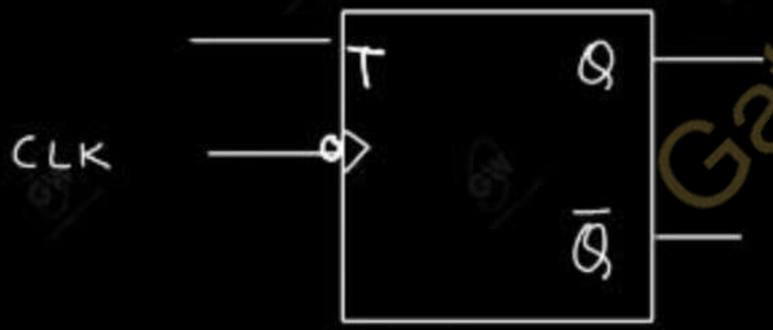
$$Q_{n+1} = \bar{T}Q_n + T\bar{Q}_n$$

Gateway Classes

Negative edge Triggered T Flip Flops

T flip-flop operates with only negative clock transitions.





	CLK	T	Q_n Present state Q_n	Q_{n+1} Next State (Q_{n+1})
Flip Flop disabled	0	x	Q_n	Q_n
	1	x	Q_n	Q_n
	↑	x	Q_n	Q_n
Flip flop Enabled for -ve Edge	↓	0	0	0
	↓	0	1	1
	↓	1	0	1
	↓	1	1	0

Gateway Classes

Excitation Table

An excitation table shows the required inputs of a flip-flop to make a desired transition from the present state (Q_n) to the next state (Q_{n+1}).

Excitation Table for SR Flip Flop

Truth Table

S	R	Q_n Present State Q_n	Q_{n+1} Next State (Q_{n+1})
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	0	x

Excitation Table →

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Gateway Classes

Excitation Table for D Flip Flop

Truth Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Gateway Classes

Excitation Table for JK Flip Flop

Truth Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Gateway Classes

Excitation Table for T Flip Flop

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Gateway Classes

AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-3 Lec-3

Gateway Classes



Avinash Sir

Today's target

- Master Slave FF
- Flip Flop Conversion
- PYQ

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- Sequential logic design: Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- Applications of Flip Flops: ripple and synchronous counters, Ring counter, Johnson counter.
- shift registers: SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- Finite state machines: Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

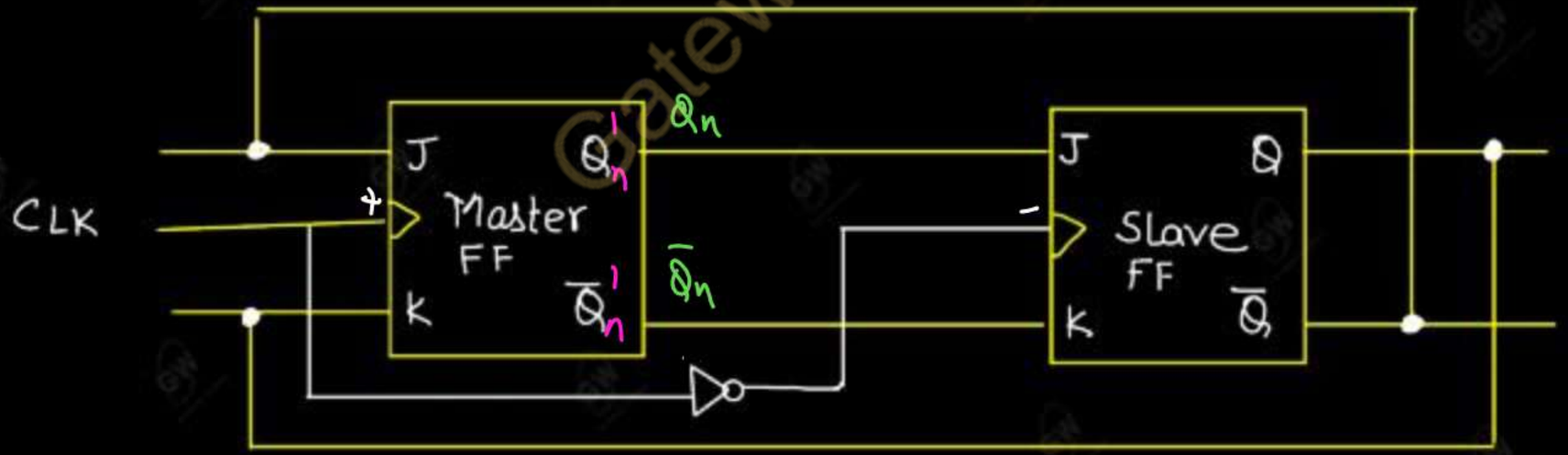
Master Slave Flip Flop

AKTU 2021-22

- Master-slave JK flip-flop is designed to eliminate the race around condition in JK flip-flop
- The first flip-flop is called the master, and it is driven by the positive clock cycle.
- The second flip-flop is called the slave, and it is driven by the negative clock cycle.
- During the positive clock cycle, master flip-flop gives the intermediate output but slave flip-flop will not give the final output.



- During the negative clock cycle, slave flip-flop gets activated and copies the previous output of the master flip-flop and produces the final output.



Gateway Classes

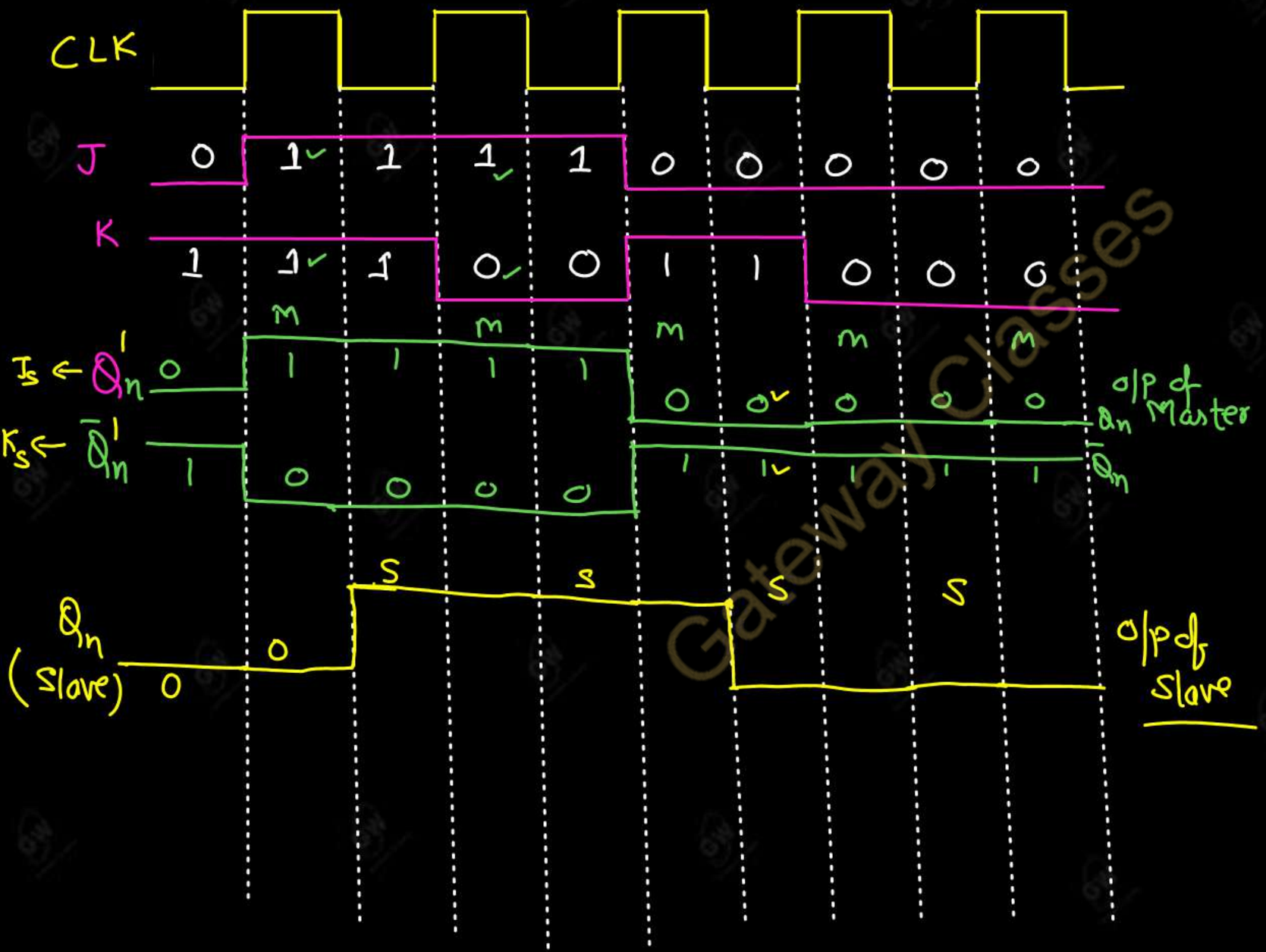
Master Slave JK Flip Flop Operation

Master flip flop responds before the slave flip flop.

- When J = 0 and K = 0, both JK flip flops remains inactive and hence the output Q remains unchanged. This is called Hold State of the master-slave JK flip flop.
- When J = 0 and K = 1, the output Q' of the master flip flop is high and goes to the input K of the slave flip flop. The clock signal forces the slave flip flop to reset. Therefore, the slave flip flop has the same output has the master flip flop, i.e., high Q' and low Q.
- When J = 1 and K = 0, the output Q of the master flip flop is high and goes to the input J of the slave flip flop, the negative transition of the clock signal sets the slave flip flop. Hence, this is called the set state of the master-slave JK flip flop.
- When J = 1 and K = 1, for this input combination, the master flip flop toggles on the positive transition of the clock pulse and the slave flip flop toggles on the negative transition of the clock pulse. Hence, the problem of the race around condition of the JK flip flop is solved.

Gateway Classes

Master Slave JK Flip Flop



Truth Table

CLK	J	K	Q_{n+1}	$\bar{Q}_{n+1}$
x	x	x	Q_n	$\bar{Q}_n$
1	0	0	Q_n	$\bar{Q}_n$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\bar{Q}_n$	Q_n

Flip Flop Conversion

Each flip-flop type has its own characteristic table (how inputs affect output).To convert one type to another:

- Write the characteristic table of the desired flip-flop.
- Write the excitation table of the given flip-flop.
- Compare both to find the required input combinations.
- Simplify using K-maps to get excitation equations.

Gateway Classes

Flip Flop Conversion From SR to D

Required — Converted from

D	Q_n	Q_{n+1}	S	R
0	0	0	0	x
1	0	1	1 ✓	0
0	1	0	0	1
1	1	1	x ✓	0

Truth Table — Excitation Table

S ↓

D \ Q_n	0	1
0		
1	1	X

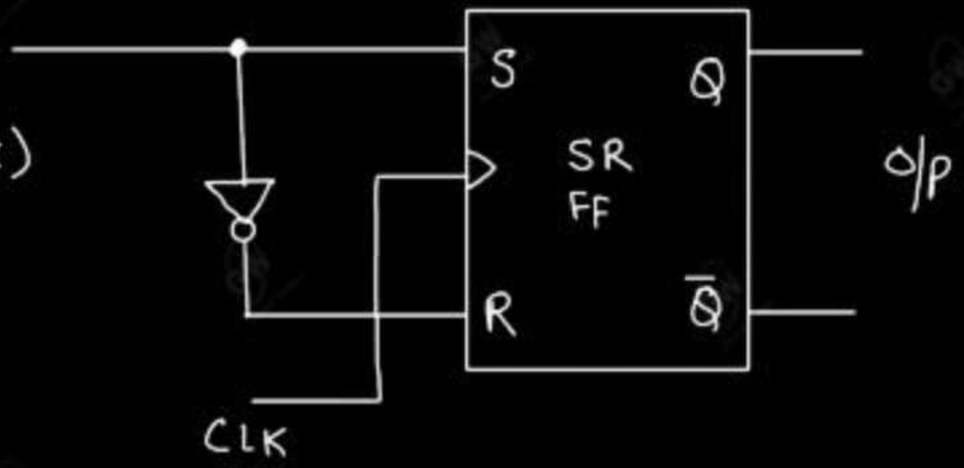
$S = D$

R ↓

D \ Q_n	0	1
$\bar{D}$ 0	X	1
D 1		

$R = \bar{D}$

Logic Diagram



"SR Flip flop to D FF"

GatewayClasses

Flip Flop Conversion From JK to T

Require → Convert ↓

T	Q_n	Q_{n+1}	J	K
0	0	0	0	x
1	0	1	1	x
1	1	0	x	1
0	1	1	x	0

Truth Table for T

Excitation Table for JK

J

T \ Q_n	0	1
0		x
1	1	x

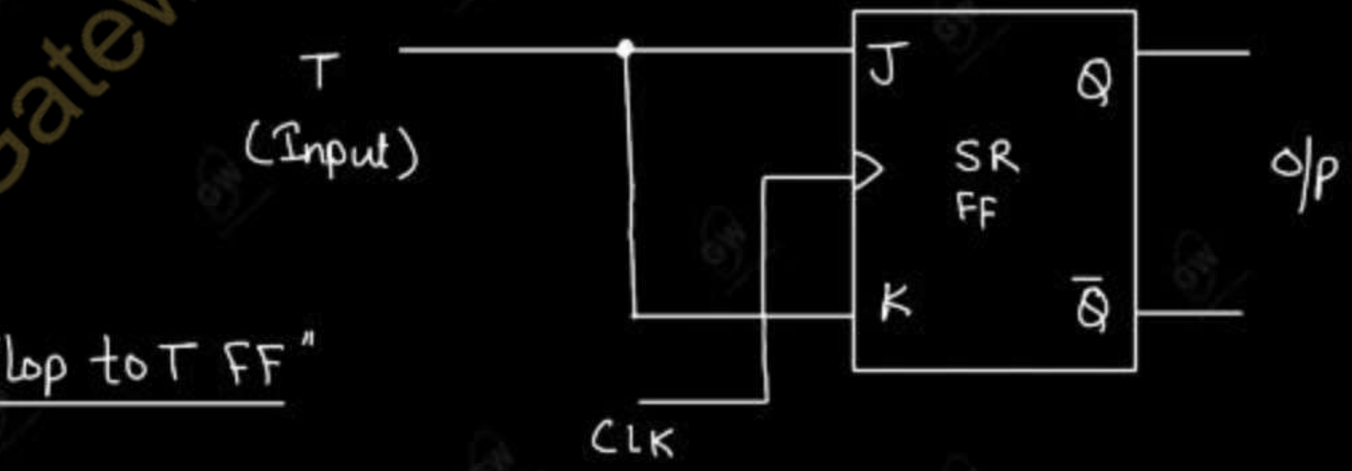
$J = T$

K

T \ Q_n	0	1
0	x	
1	x	1

$K = T$

Logic Diagram



"JK Flip flop to T FF"

Gateway Classes

Flip Flop Conversion From T to D

D	Q_n	Q_{n+1}	T
0	0	0	0
1	0	1	1
0	1	0	1
1	1	1	0

T.T

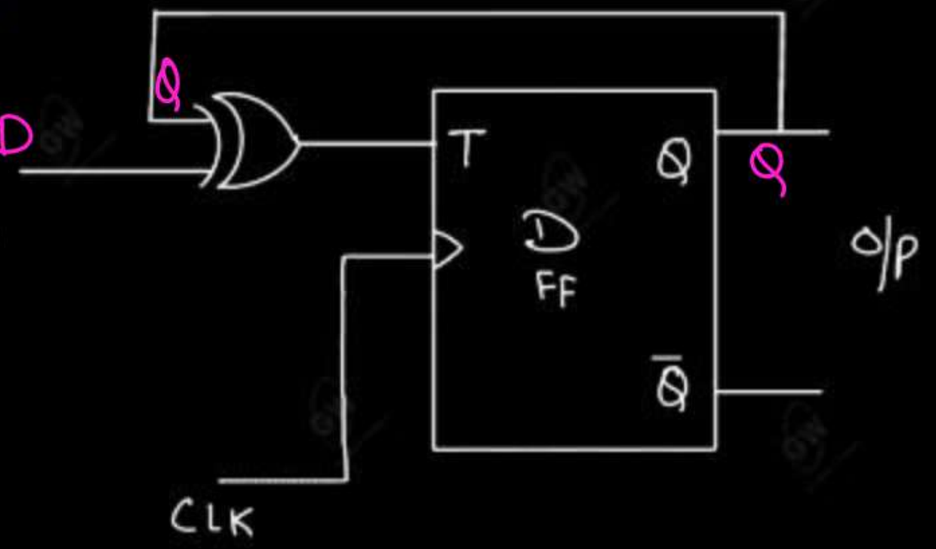
E.T.

T

D \ Q_n	0	1
0		1
1	1	

$T = \bar{D}Q_n + D\bar{Q}_n = D \oplus Q_n$

Logic Diagram



"D Flip flop to T FF"

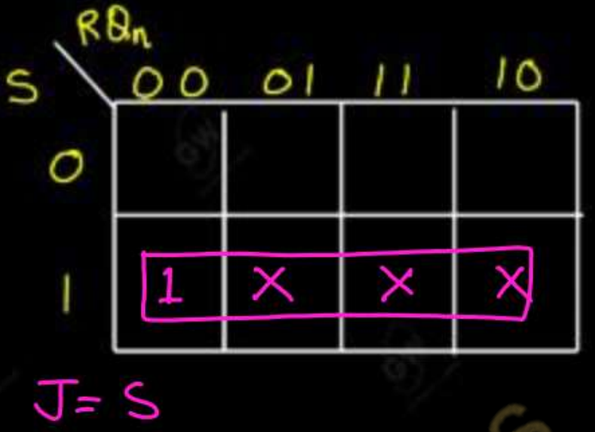
Gateway Classes

Flip Flop Conversion From JK to SR

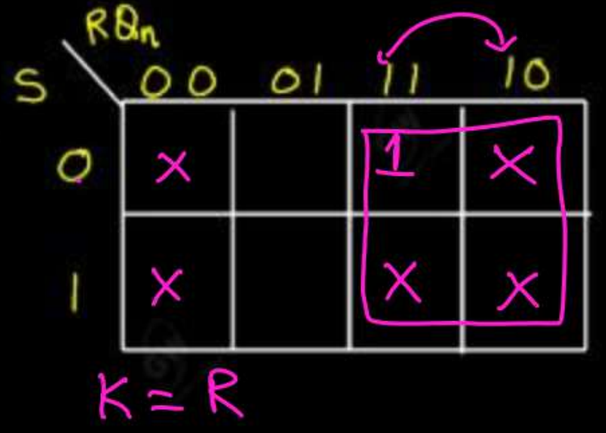
S	R	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
0	1	0	0	0	x
1	0	0	1	1	X
1	1	0	1	x	X
0	0	1	0	X	0
0	1	1	0	X	1
1	0	1	1	x	0
1	1	1	1	X	x

T·T SR

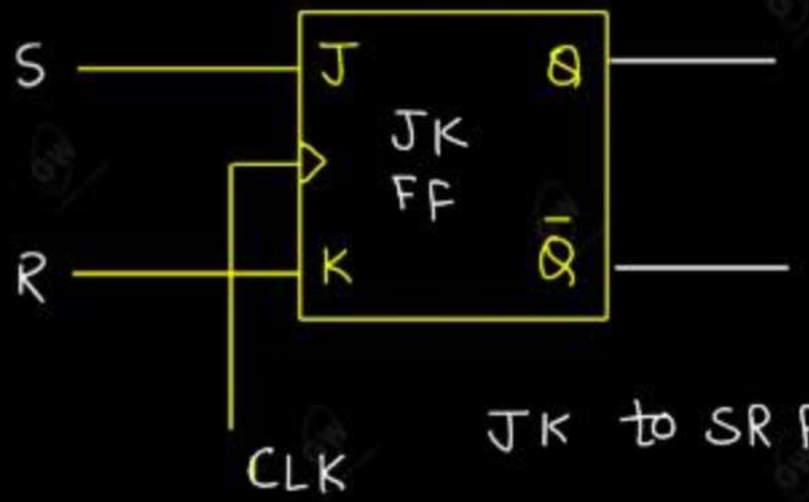
E·T JK



J = S



K = R



JK to SR FF

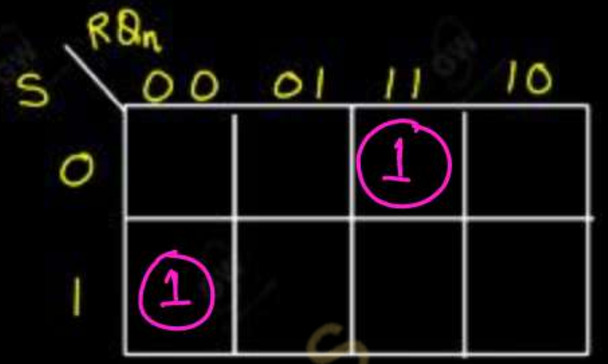
Gateway Classes

Flip Flop Conversion From T to SR

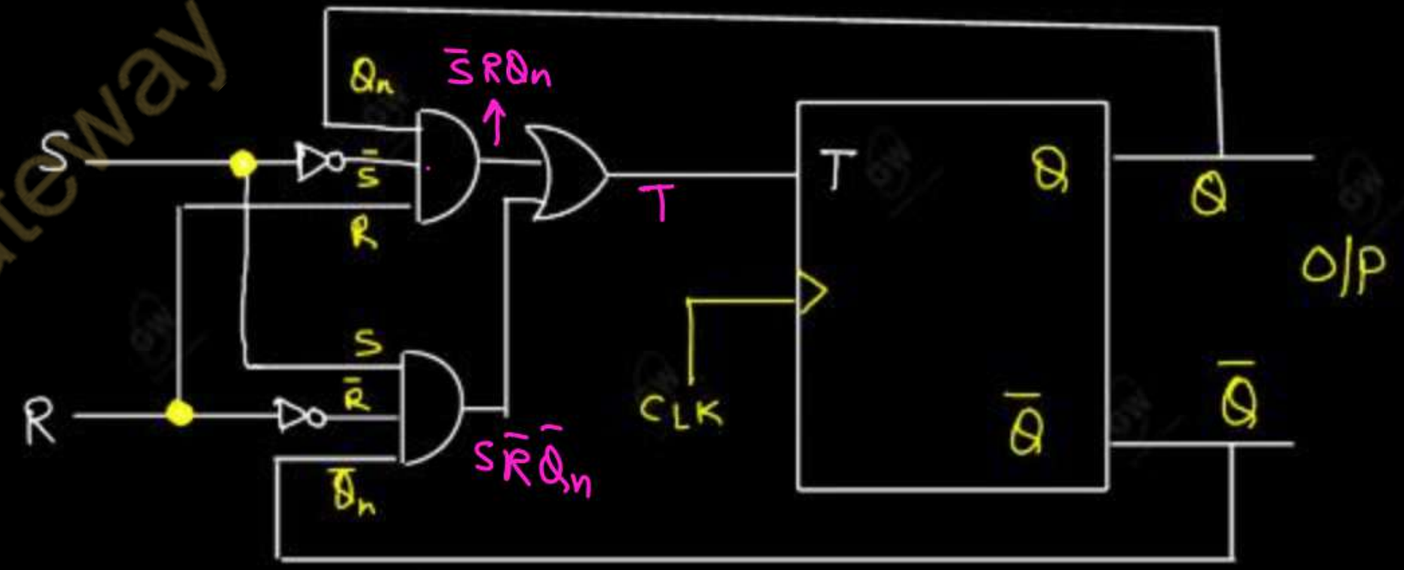
S	R	Q_n	Q_{n+1}	T
0	X	0	0	0
1	0	0	1	1 ✓
0	1	1	0	1 ✓
X	0	1	1	0

T·T(SR)

(E·T)T



$T = S\bar{R}\bar{Q}_n + \bar{S}RQ_n$



Gateway Classes

AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-3 Lec-4



Avinash Sir

Today's target

- Shift Registers
- Bidirectional Shift Registers
- Universal Shift Registers
- PYQ

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

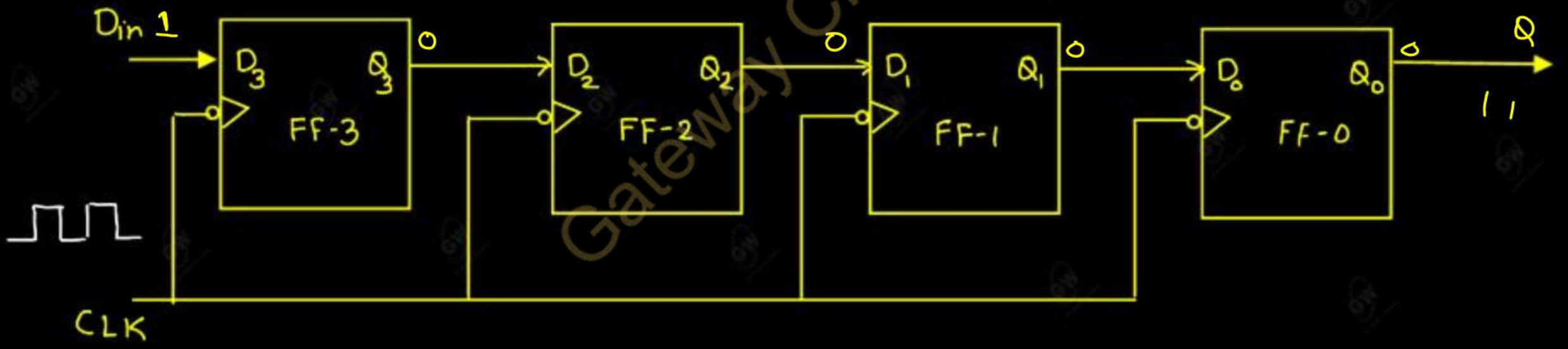
Shift Registers

- A Flip-flop is a 1 bit memory cell which can be used for storing the digital data. To increase the storage capacity in terms of number of bits, you can use a group of flip-flops. Such a group of flip-flops is known as a Register. The n-bit register will consist of n number of flip-flop(s) and it is capable of storing an n-bit word.
- A shift register is a type of register that allows such data transfers. Shift register has 4 modes of operations.
  - Serial-in serial-out SISO
  - Serial-in parallel-out SIPO
  - Parallel-in serial-out PISO
  - Parallel-in parallel-out PIPO

Gateway Classes

Serial-in serial-out (SISO)

Let all the flip-flops be initially in the reset condition i.e. Q3 = Q2 = Q1 = Q0 = 0. If an entry of a four-bit binary number 1 1 1 1 is made into the register, this number should be applied to D_{in} bit with the LSB bit applied first. The D input of FF-3 i.e. D3 is connected to serial data input D_{in}. The output of FF-3 i.e. Q3 is connected to the input of the next flip-flop i.e. D2, and so on.



Gateway Classes

- On the first falling edge of the clock, the FF-3 is set, and stored word in the register is Q3 Q2 Q1 Q0 = 1000.
- Apply the next bit to Din. So Din = 1. As soon as the next negative edge of the clock gets triggered, FF-2 will set and the stored word change to Q3 Q2 Q1 Q0 = 1100.
- Apply the next bit to be stored i.e. 1 to Din. Apply the clock pulse. As soon as the third negative clock edge gets triggered, FF-1 will be set and output will get modified to Q3 Q2 Q1 Q0 = 1110.
- Similarly with Din = 1 and with the fourth negative clock edge arriving, the stored word in the register is Q3 Q2 Q1 Q0 = 1111.

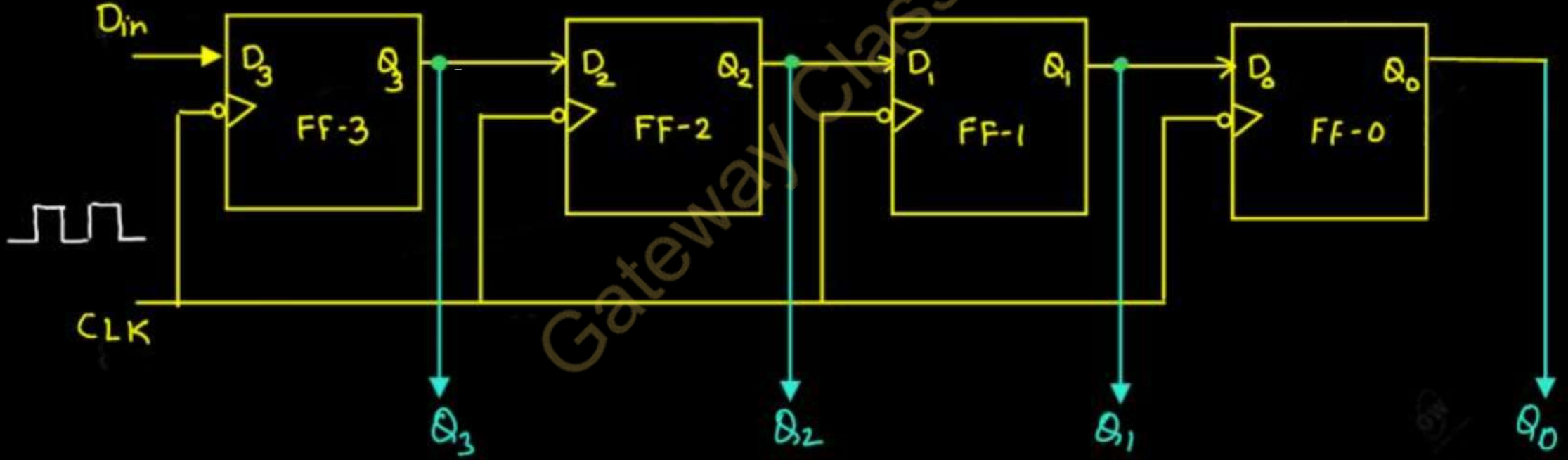
CLK	$D_{in}=Q_3$	$Q_3=D_2$	$Q_2=D_1$	$Q_1=D_0$	Q_0
X	–	0	0	0	0
1 ↓	1 →	1	0	0	0
2 ↓	1 →	1	1	0	0
3 ↓	1 →	1	1	1	0
↓	1 →	1	1	1	1

Direction of data travel →

Gateway Classes

Serial-in parallel-out (SIPO)

- In such types of operations, the data is entered serially and taken out in parallel fashion.
- Data is loaded bit-by-bit. The output(s) are disabled as long as the data is loading.
- As the data loading gets completed, all flip-flops contain their required data. The output(s) are enabled so that all the loaded data is made available over all the output lines at the same time.



Gateway Classes

- 4 clock cycles are required to load a four-bit word. Hence the speed of operation of SIPO mode is the same as that of the SISO mode.

Parallel-in serial-out

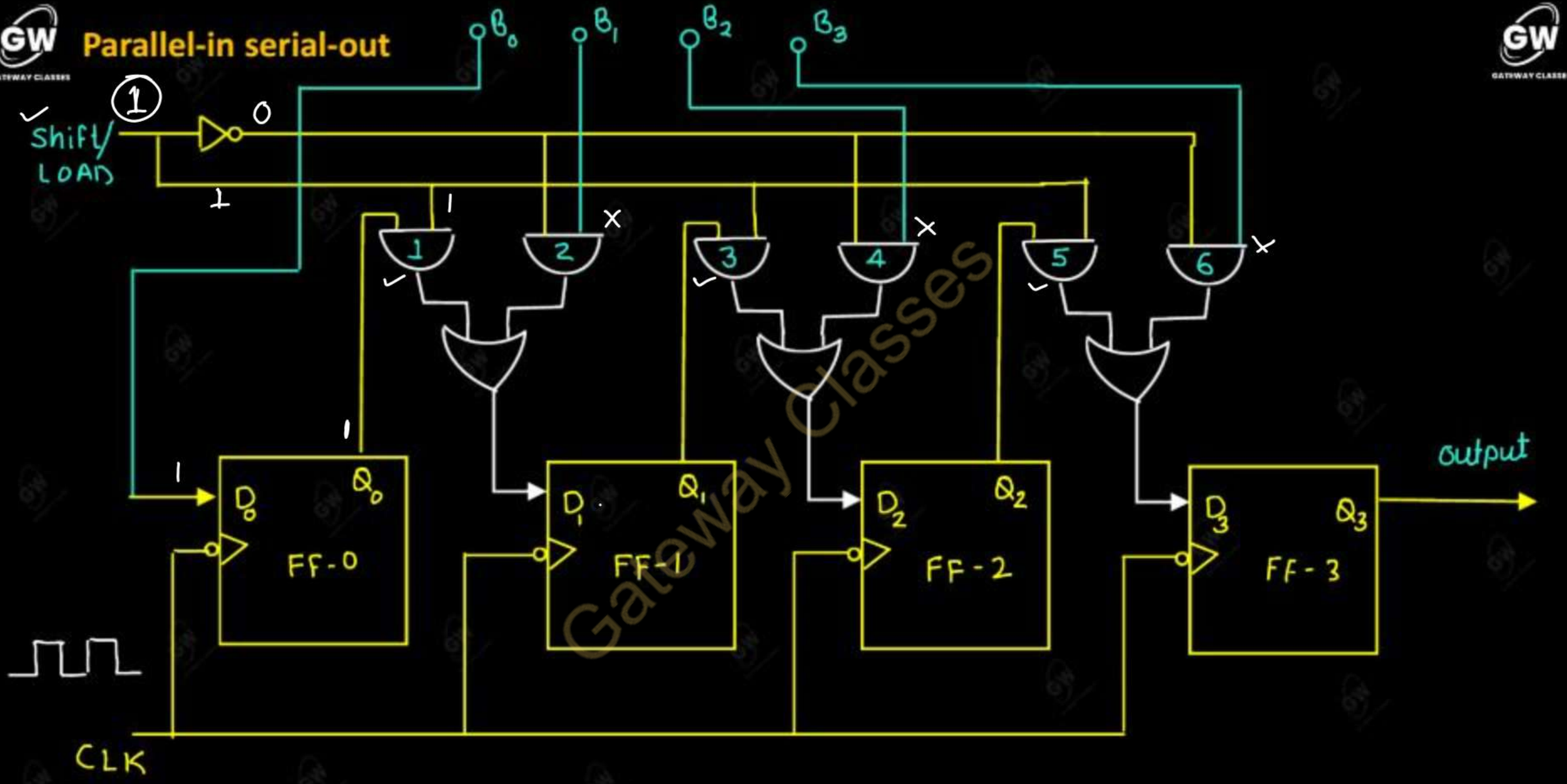
- Data bits enter in a parallel fashion.
- The circuit, shown below, is a four-bit parallel-in serial-out register.
- Output of the previous flip Flop is connected to the input of the next one via a combinational circuit.
- The binary input data bits B0, B1, B2, B3 are applied through the same combinational logic circuit.
- There are two modes in which this circuit can work, namely - shift mode and load mode.

Load mode:- When the shift/load bar line is low (0), the AND gates 2, 4 and 6 become active, and they will pass B_1, B_2, B_3 bits to the corresponding flip-flops. On –ve edge of the clock, the binary inputs B_0, B_1, B_2, B_3 will get loaded into the corresponding flip-flops. Thus, the parallel loading takes place.

Shift mode:- When the shift/load bar line is high (1), the AND gates 2, 4 and 6 become inactive. AND gates 1,3 and 5 become active. Therefore the shifting of data takes place from left-to-right bit-by-bit on the application of clock pulses. Thus, the parallel-in serial-out operation takes place.

Gateway Classes

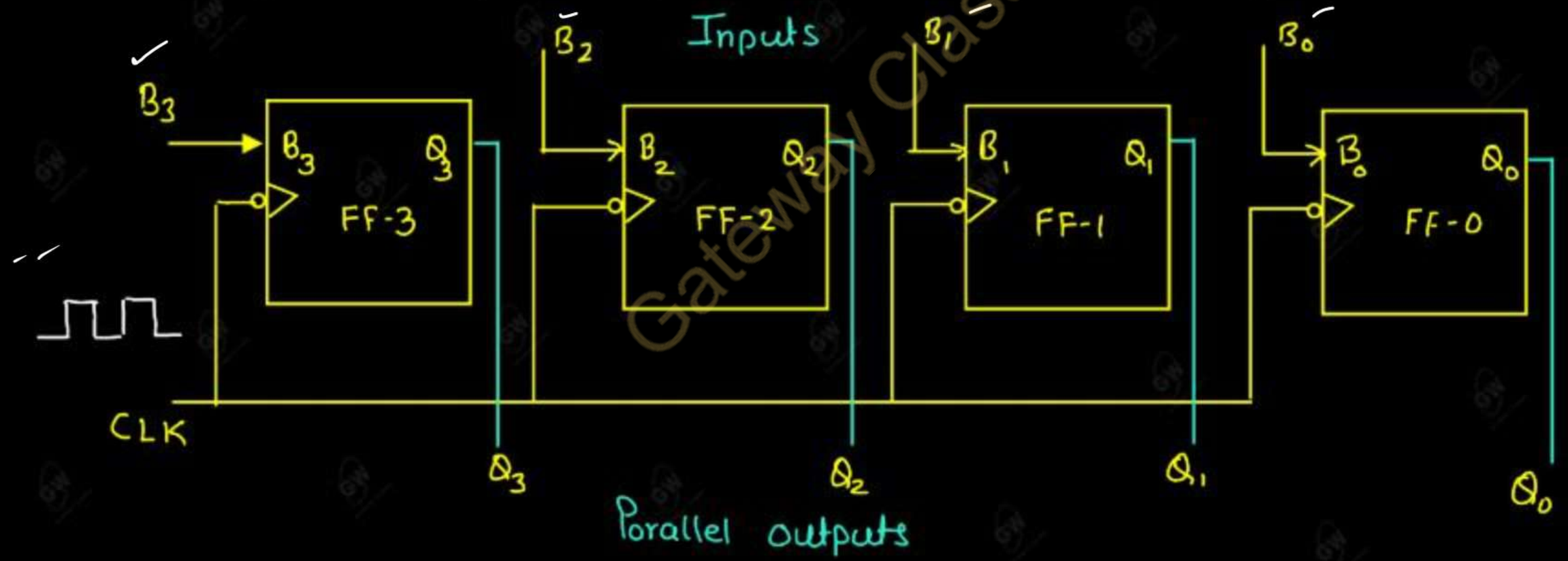
Parallel-in serial-out



Gateway Classes

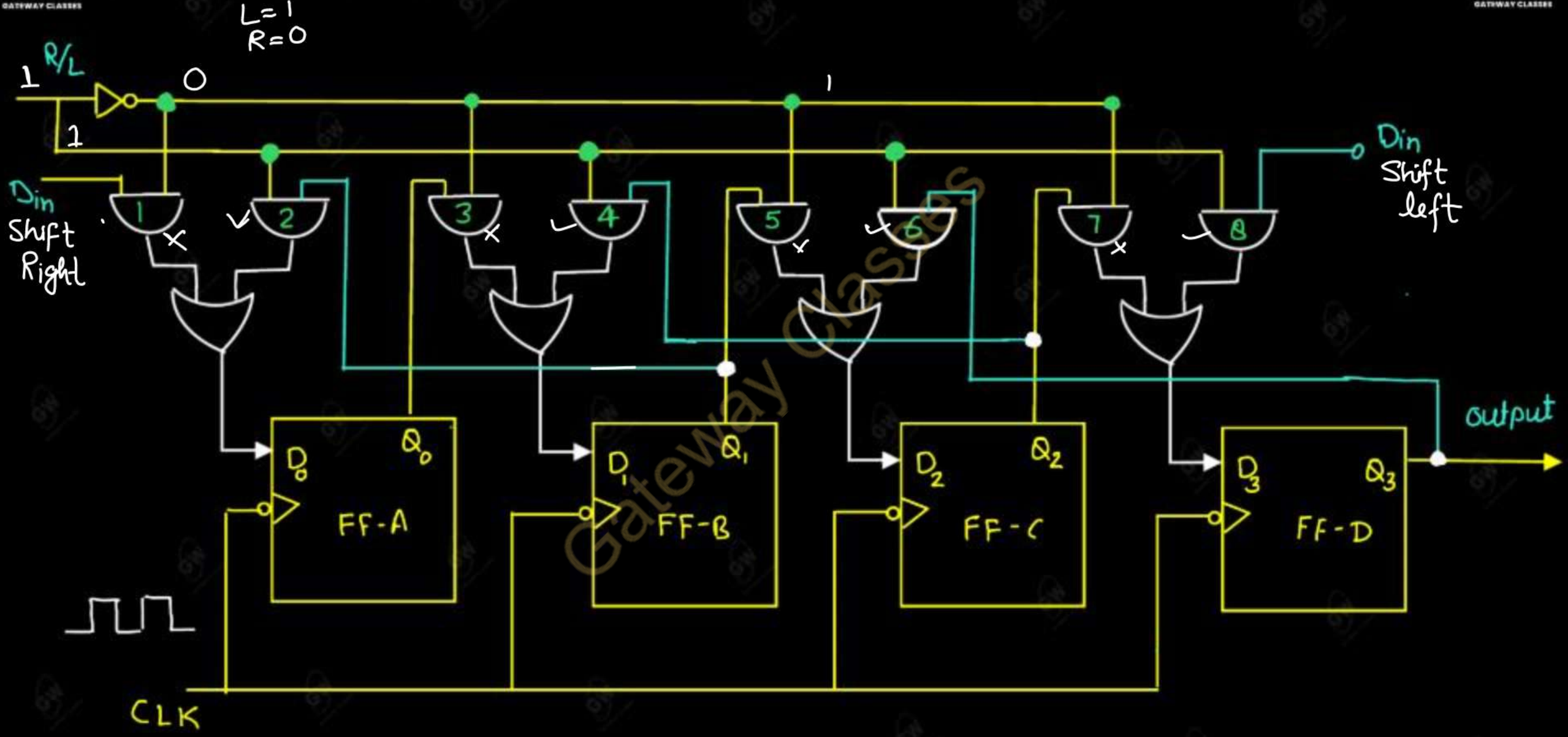
Parallel-in parallel-out

Here, the 4-bit binary data inputs B0, B1, B2, B3 are applied to the data inputs D0, D1, D2, D3, respectively, of the four flip-flops. When a negative edge of the clock is triggered, then the flip-flops get loaded with the input binary bits simultaneously. The loaded bits appear at the output side, simultaneously, as well. Only the clock pulse is essential to load all the binary bits.



Gateway Classes

Bidirectional Shift Register



Gateway Classes

Bidirectional Shift Register

Case 1: Shift-Right Operation

When the control signal R/L' is HIGH, then the AND gates 1, 3, 5, and 7 are enabled, and the AND gates 2, 4, 6, and 8 are disabled. The output of the flip-flop A is connected to the input of the flip-flop B, the output of the flip-flop B is connected to the input of the flip-flop C, and the output of the flip-flop C is connected to the input of the flip-flop D. Hence, when a clock signal occurs, the data bits are shifted one place to the right.

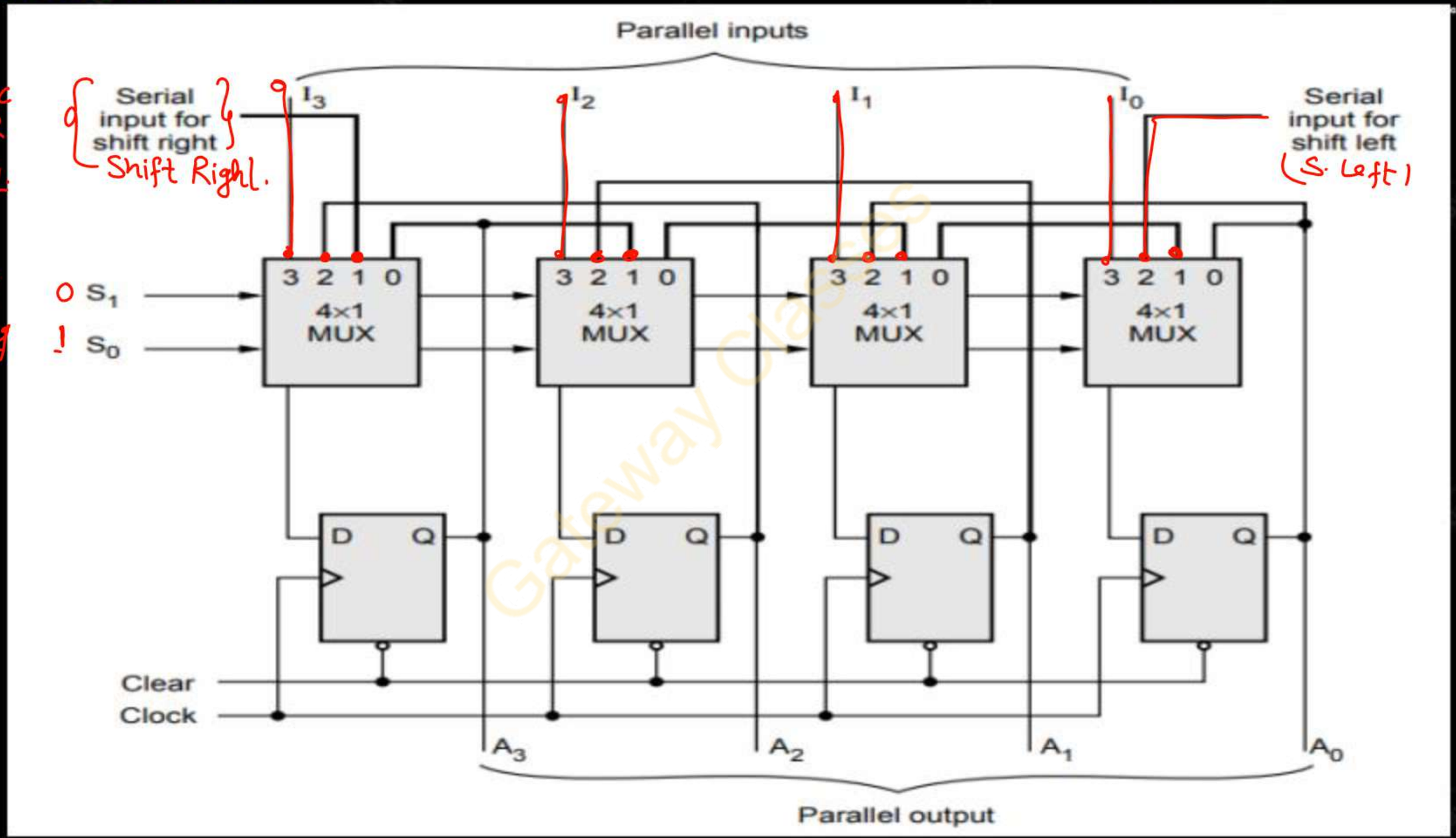
Case 2: Shift-Left Operation

When the control signal R/L' is LOW, then the AND gates 2, 4, 6, and 8 are enabled, and the AND gates 1, 3, 5, and 7 are disabled. The output Q of each flip-flop connected to the D input of the following flip-flop. Thus, when a clock signal occurs, the data bits are shifted one place to the left.

Gateway Classes

Universal Register

AKTU -2022-23



S0 S1
0 0 → NC
0 1 → SR
1 0 - S.L
1 1 - .
Parallel loading

Gateway Classes

Universal Shift Register

- If the register has both shifts (right shift and left shift) and parallel load capabilities, it is referred to as universal shift register.
- The four multiplexers have two common selection inputs S1 and S0, and they select appropriate input for D flip-flop.
- When $S_1S_0 = 00$, I_0 is selected ,no change in the register value.
- When $S_1S_0 = 01$, I_1 is selected, operates as a right shift register.
- When $S_1S_0 = 10$, I_2 is selected, operates as a left shift register.
- Finally, when $S_1S_0 = 11$, it is a parallel load operation.

Mode control		Register operation
S_1	S_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Mode control and register operation

Gateway Classes

AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design



Unit-3 Lec-5

Today's target

- Ripple and synchronous counters,
- Ring counter
- Johnson counter
- PYQ

Avinash Sir

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

Types of Counters

- 1. Asynchronous counter ⇒ Ripple counter, serial (or) series (up/down)
- 2. Synchronous counter ⇒ Parallel counter

Asynchronous → CLK Pulse to first ff.

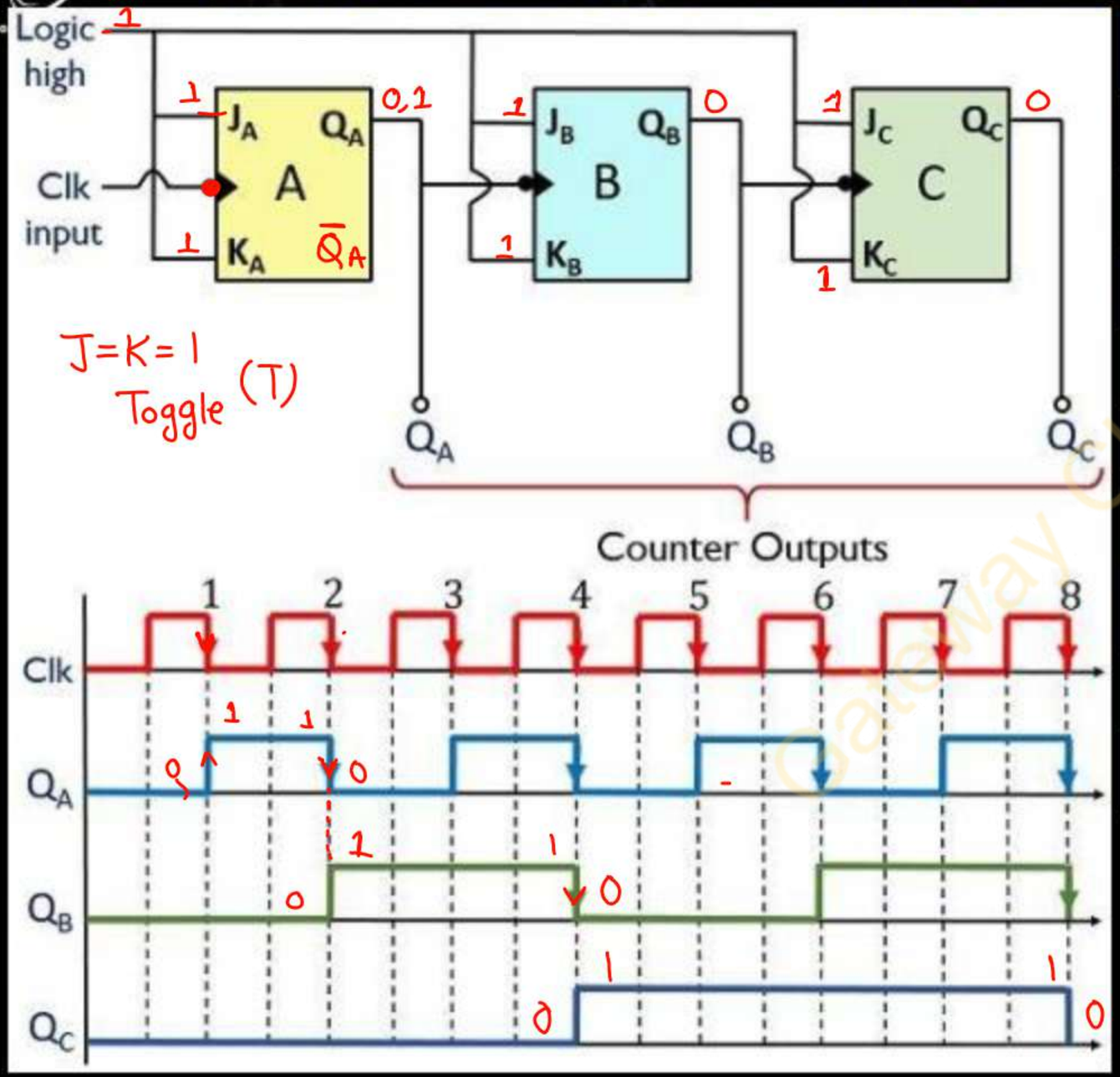
Synchronous → CLK Pulse to all ff.

Gateway Classes

Synchronous Counter	Asynchronous Counter
Common clock applied to all flip flops.	main clock is only applied to the first flip flop and then for rest of flip flops the output of previous flip flop is taken as a clock.
Synchronous Counter is faster in operation	Asynchronous Counter is slower
Synchronous Counter is also called Parallel Counter.	Asynchronous Counter is also called Serial Counter.
designing as well implementation are complex due to increasing the number of states.	designing as well as implementation is very easy.
operate in any desired count sequence.	operate only in fixed count sequence (UP/DOWN).
propagation delay is less.	there is high propagation delay.

Gateway Classes

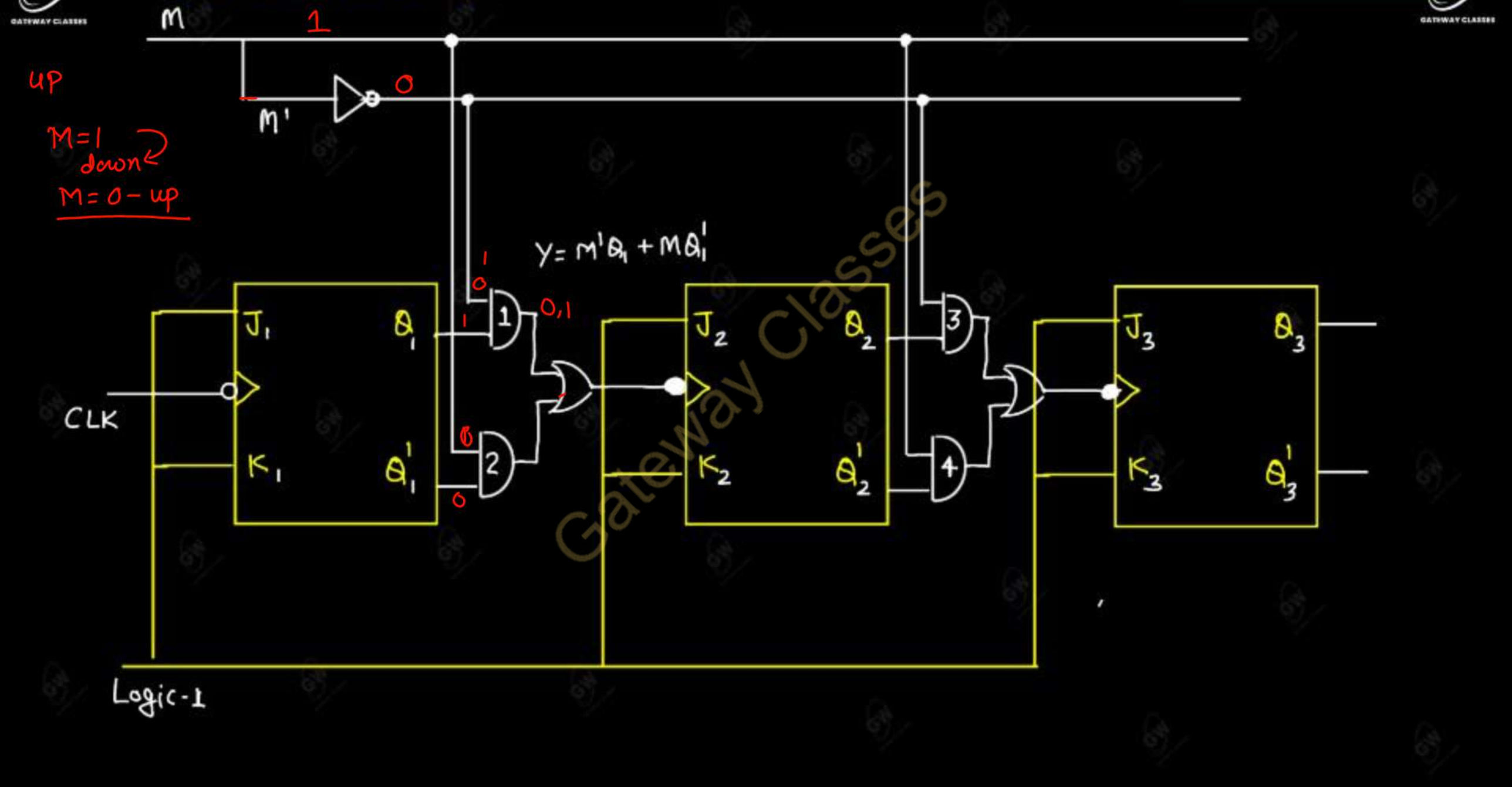
3-Bit Asynchronous counter ⇒ Ripple counter, serial (or) series



Clock	Qc	QB	QA	Decimal
Intiial	0	0	0	0
1st falling Edge	0	0	1	1
2nd falling Edge	0	1	0	2
3rd falling Edge	0	1	1	3
4th falling Edge	1	0	0	4
5th falling Edge	1	0	1	5
6th falling Edge	1	1	0	6
7th falling Edge	1	1	1	7
8th falling Edge	0	0	0	0

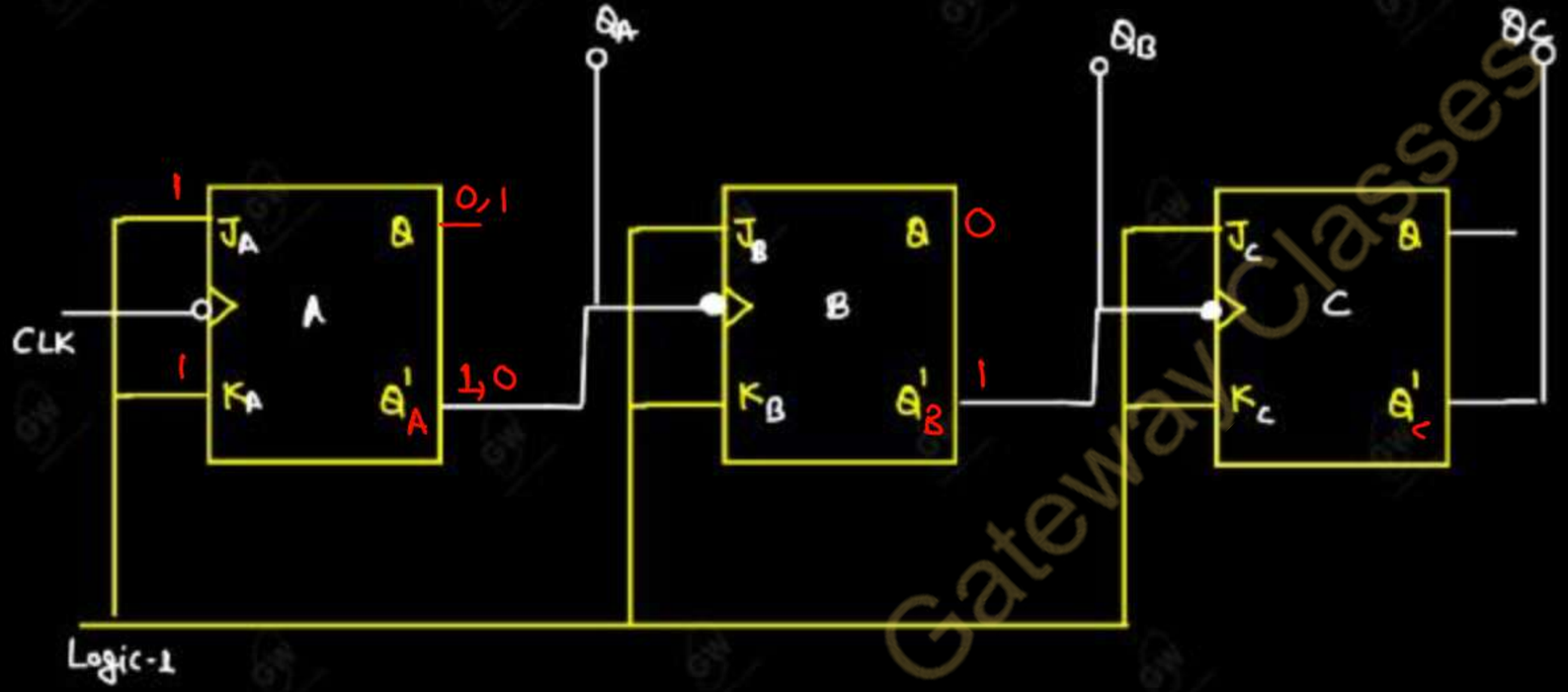
3 bit UP/Down Counter

AKTU-2022-23



Gateway Classes

Down Counter



CLK	Q_C	Q_B	Q_A	Dec.
1 ↓	1	1	1	7
2 ↓	1	1	0	6
3 ↓	1	0	1	5
4 ↓	1	0	0	4
5 ↓	0	1	1	3
6 ↓	0	1	0	2
7 ↓	0	0	1	1
8 ↓	0	0	0	0

Gateway Classes

4- Bit Synchronous Counter (UP)

0000 — 1111

n = 4

ff = 4

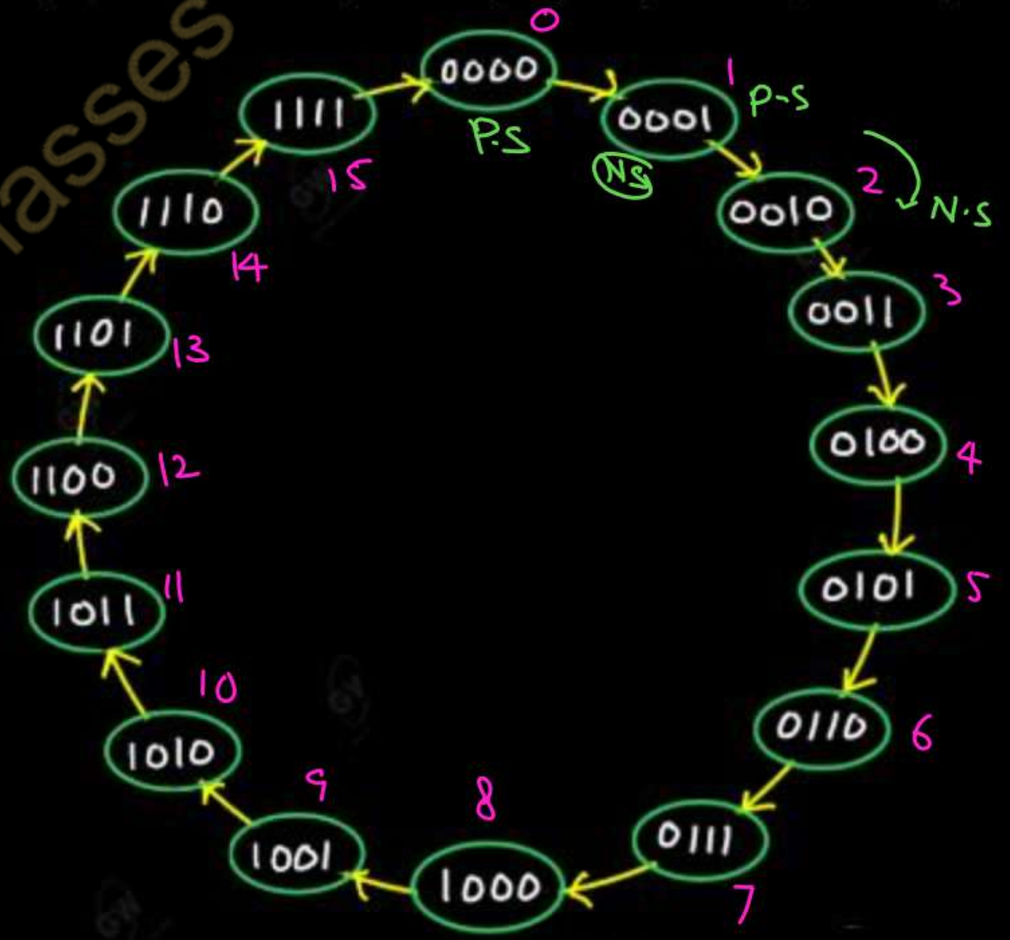
2^4 = 16 state

Step 1: Find the number of flip flops.

for a 4 bit counter, 4 flip flops(n=4) are needed

Number of states = $2^n = 2^4$ = 16states (0000, 0001, 0010,0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111)

Step 3: Draw state diagram for the counter.



Gateway Classes

Step 4: Obtain excitation table for the counter.

excitation table for Counter

CLK	Present state Q_D	Q_C	Q_B	Q_A	Next state Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A	
1	0	0	0	0	0	0	0	1	0	x	0	x	0	x	1	x	0
2	0	0	0	1	0	0	1	0	0	x	0	x	1	x	x	1	1
3	0	0	1	0	0	0	1	1	0	x	0	x	x	0	1	x	2
4	0	0	1	1	0	1	0	0	0	x	1	x	x	1	x	1	3
5	0	1	0	0	0	1	0	1	0	x	x	0	0	x	1	x	4
6	0	1	0	1	0	1	1	0	0	x	x	0	1	x	x	1	5
7	0	1	1	0	0	1	1	1	0	x	x	0	x	0	1	x	6
8	0	1	1	1	1	0	0	0	1	x	x	1	x	1	x	1	7
9	1	0	0	0	1	0	0	1	x	0	0	x	0	x	1	x	8
10	1	0	0	1	1	0	1	0	x	0	0	x	1	x	x	1	9
11	1	0	1	0	1	0	1	1	x	0	0	x	x	0	1	x	10
12	1	0	1	1	1	1	0	0	x	0	1	x	x	1	x	1	11
13	1	1	0	0	1	1	0	1	x	0	x	0	0	x	1	x	12
14	1	1	0	1	1	1	1	0	x	0	x	0	1	x	x	1	13
15	1	1	1	0	1	1	1	1	x	0	x	0	x	0	1	x	14
16	1	1	1	1	0	0	0	0	x	1	x	1	x	1	x	1	15

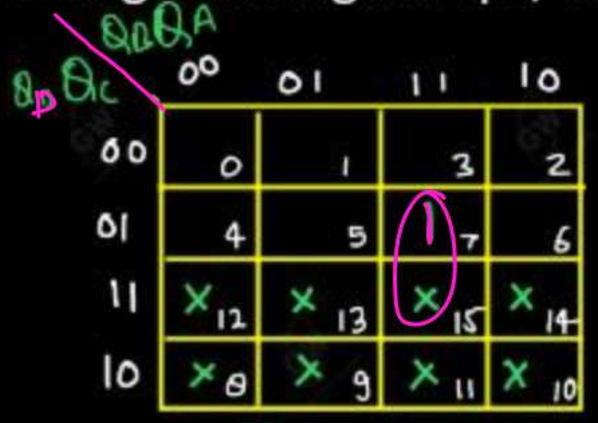
excitation table for JK flip flop

P.S Q_n	N.S Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

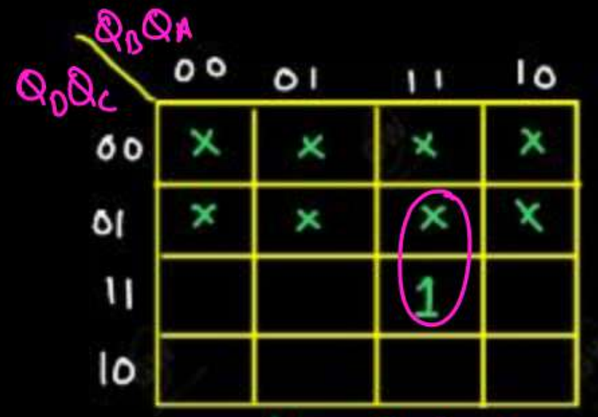
Gateway Classes

Step 5: Derive the flip flop input functions.

Using Karnaugh maps, the input functions for the 4 flip flops are derived.



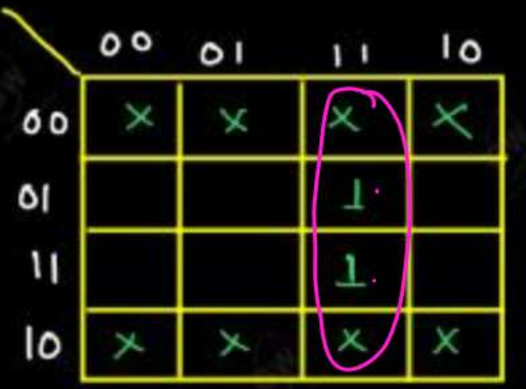
$J_D = Q_A Q_B Q_C$



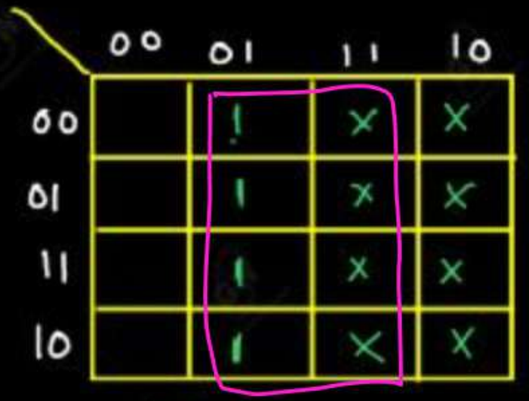
$K_D = Q_A Q_B Q_C$



$J_C = Q_A Q_B$



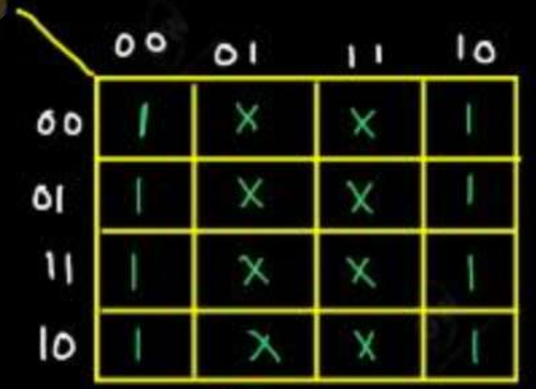
$K_C = Q_A Q_B$



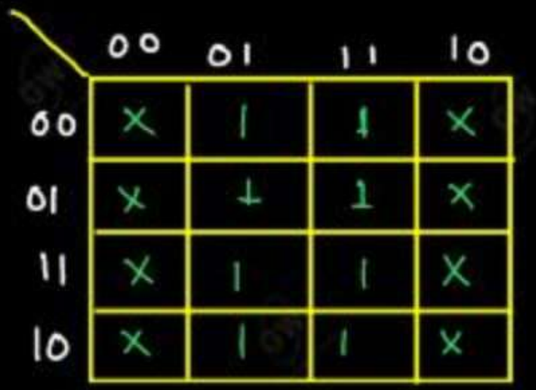
$J_B = Q_A$



$K_B = Q_A$



$J_A = 1$

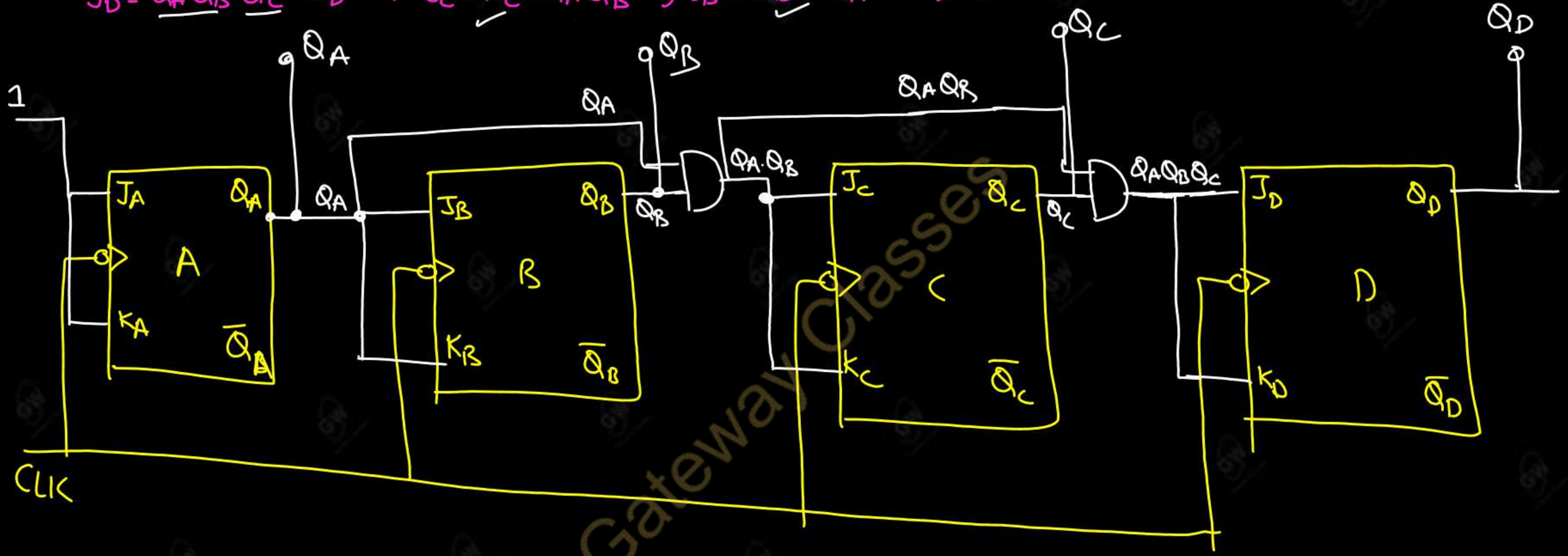


$K_A = 1$

Gateway Classes

Step 6: Draw the logic diagram of the counter.

$J_D = Q_A Q_B Q_C = K_D$, $J_C = K_C = Q_A Q_B$, $J_B = K_B = Q_A$, $J_A = K_A = 1$



Gateway Classes

3- Bit Synchronous Counter (UP)

$2^n = 8$

000 — 111 → 8 state

Step 1: Find the number of flip flops.

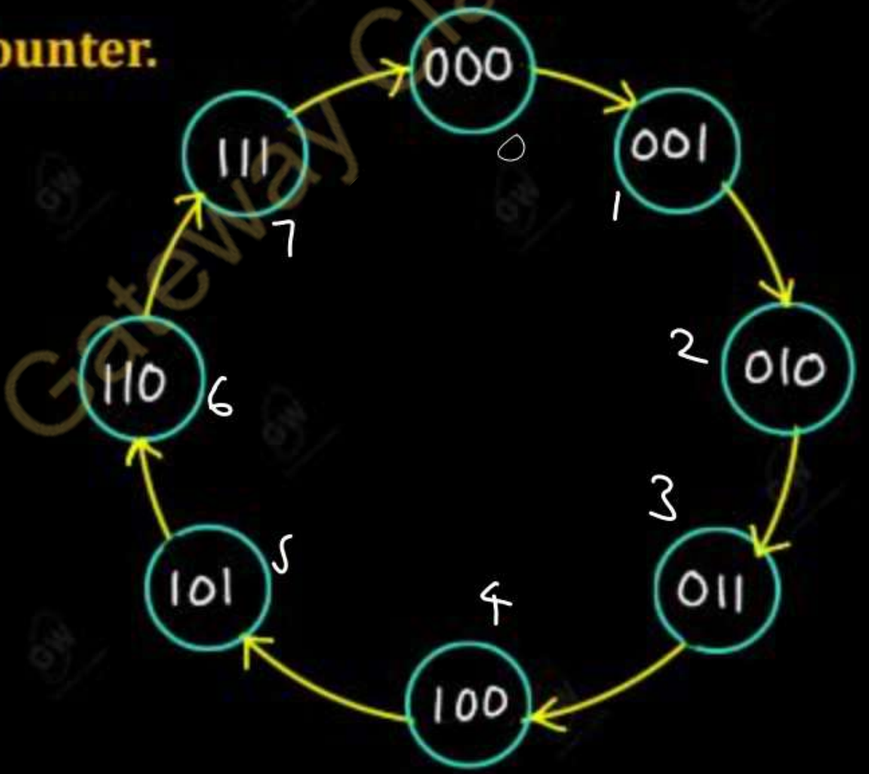
for a 3 bit counter, 3 flip flops(n=3) are needed

Number of states = $2^n = 2^3 = 8$ states(000, 001, 010, 011, 100, 101, 110, 111)

Step 2: Choose the type of flip flop.

Since the type of flip flop is given in the problem, let us use JK flip flops.

Step 3: Draw state diagram for the counter.



Gateway Classes

Step 4: Obtain excitation table for the counter.

excitation table for Counter

Clock	Present State			Next State			Flip flop Inputs					
	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
1	0	0	0	0	0	1	0	X	0	X	1	X
2	0	0	1	0	1	0	0	X	1	X	X	1
3	0	1	0	0	1	1	0	X	X	0	1	X
4	0	1	1	1	0	0	1	X	X	1	X	1
5	1	0	0	1	0	1	X	0	0	X	1	X
6	1	0	1	1	1	0	X	0	1	X	X	1
7	1	1	0	1	1	1	X	0	X	0	1	X
8	1	1	1	0	0	0	X	1	X	1	X	1

excitation table for JK flip flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 5: Derive the flip flop input functions.

Using Karnaugh maps, the input functions for the 3 flip flops are derived.

For J_C

Q_C \ Q_BQ_A	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_C = Q_BQ_A$ $Q_A \cdot Q_B = J_C$

For K_C

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	X	X
1	0	0	1	0

$K_C = Q_BQ_A$

For J_B

Q_C \ Q_BQ_A	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$J_B = Q_A$

For K_B

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	1	0
1	X	X	1	0

$K_B = Q_A$

For J_A

Q_C \ Q_BQ_A	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$J_A = 1$

For K_A

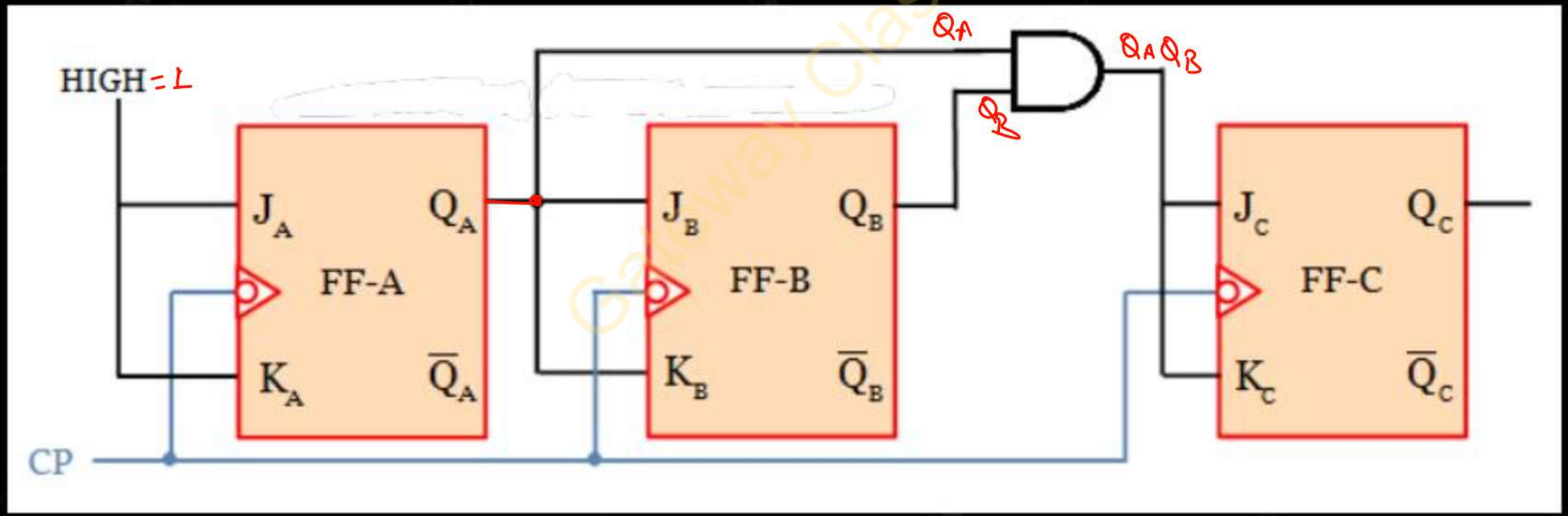
Q_C \ Q_BQ_A	00	01	11	10
0	X	1	1	X
1	X	1	1	X

$K_A = 1$

Gateway Classes

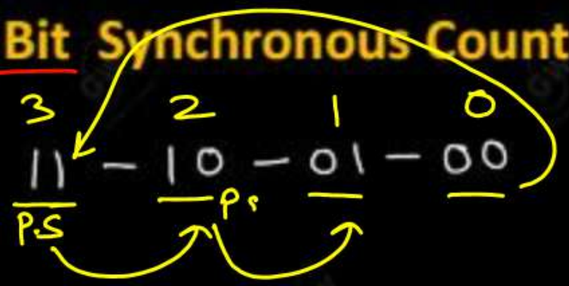
Step 6: Draw the logic diagram of the counter.

The logic diagram of the 3-bit synchronous counter is drawn as follows. Draw the 3 JK flip-flops. The common clock pulse input is given to all the flip-flops. The inputs for each flip-flop are drawn as per the logic functions derived in the previous step. $J_C = K_C = Q_A Q_B$, $J_B = K_B = Q_A$, $J_A = K_A = 1$

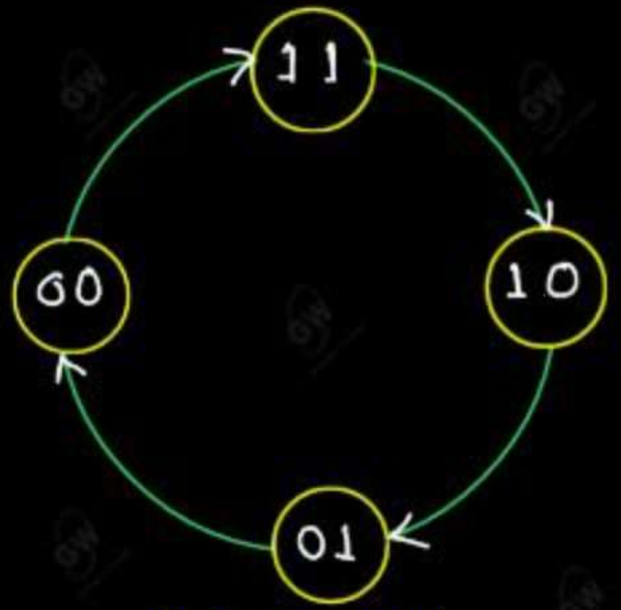


Gateway Classes

2- Bit Synchronous Counter (Down)



CLK	Present I/P		Next I/P		FF I/P				
	Q_B	Q_A	Q_{B+1}	Q_{A+1}	J_B	K_B	J_A	K_A	
1	1	1	1	0	X	0	X	1	3
2	1	0	0	1	X	1	1	X	2
3	0	1	0	0	0	X	X	1	1
4	0	0	1	1	1	X	1	X	0



Excitation Table.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Gateway Classes

2- Bit Synchronous Counter (Down)

Q_B \ Q_A	0	1
0	1 (0)	(1)
1	X (2)	X (3)

$J_B = \bar{Q}_A$ ✓

Q_B \ Q_A	0	1
0	X	X
1	1	

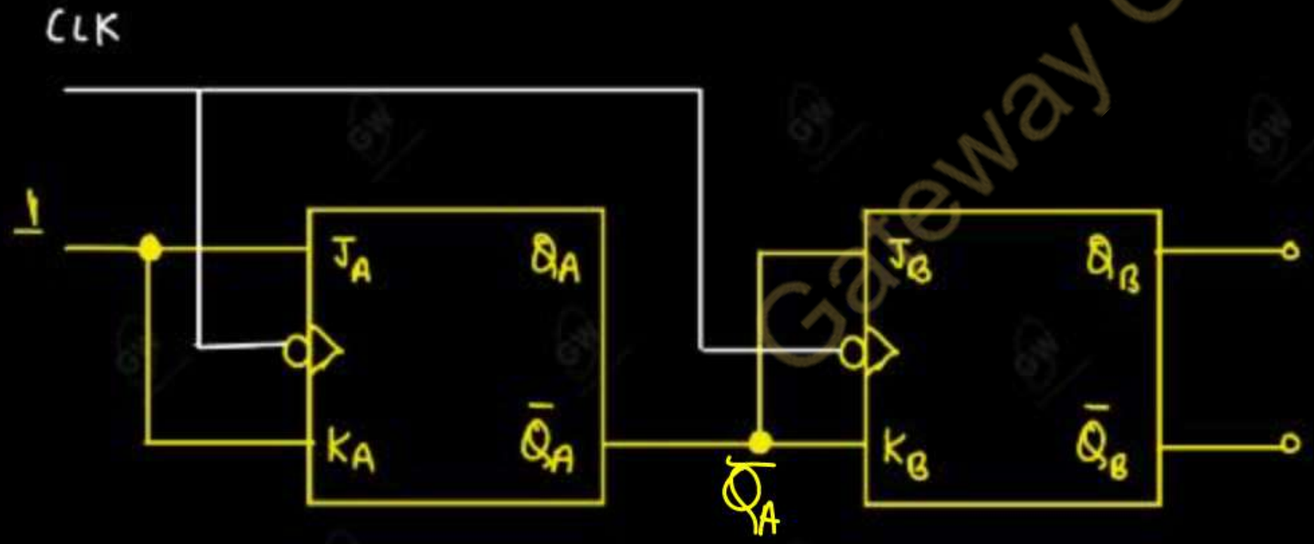
$K_B = \bar{Q}_A$

Q_B \ Q_A	0	1
0	1	X
1	1	X

$J_A = 1$

Q_B \ Q_A	0	1
0	X	1
1	X	1

$K_A = 1$



" 2 Bit Down Counter "

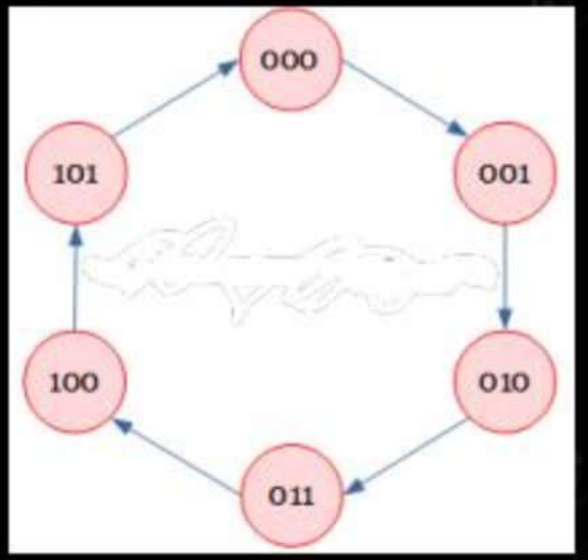
Gateway Classes

Ex. Design a MOD-6 Counter Using JK FF.

000 — 101
0,1,2,3,4,5 → 101

Mod-6 counter represents that the counter will have 6 states (001 to 110). Thus, N = 6. That is the number of flip-flops, n = 3.

The state diagram for the mod-6 counter with 6 states is drawn as below.



The excitation table for JK flip flop is given by,

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Gateway Classes

Excitation table for MOD-6 counter

Clock	Present State			Next State			Flip flop Inputs						
	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A	
1	0	0	0	0	0	1	0	X	0	X	1	X	0
2	0	0	1	0	1	0	0	X	1	X	X	1	1
3	0	1	0	0	1	1	0	X	X	0	1	X	2
4	0	1	1	1	0	0	1	X	X	1	X	1	3
5	1	0	0	1	0	1	X	0	0	X	1	X	4
6	1	0	1	0	0	0	X	1	0	X	X	1	5
-	1	1	0	X	X	X	X	X	X	X	X	X	6
-	1	1	1	X	X	X	X	X	X	X	X	X	7

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Gateway Classes

Derive the flip flop input functions.

For J_C

Q_BQ_A / Q_C	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_C = Q_BQ_A$

For K_C

Q_BQ_A / Q_C	00	01	11	10
0	X	X	X	X
1	0	1	X	X

$K_C = Q_A$

For J_B

Q_BQ_A / Q_C	00	01	11	10
0	0	1	X	X
1	0	0	X	X

$J_B = \overline{Q}_C Q_A$

For K_B

Q_BQ_A / Q_C	00	01	11	10
0	X	X	1	0
1	X	X	X	X

$K_B = Q_A$

For J_A

Q_BQ_A / Q_C	00	01	11	10
0	1	X	X	1
1	1	X	X	X

$J_A = 1$

For K_A

Q_BQ_A / Q_C	00	01	11	10
0	X	1	1	X
1	X	1	X	X

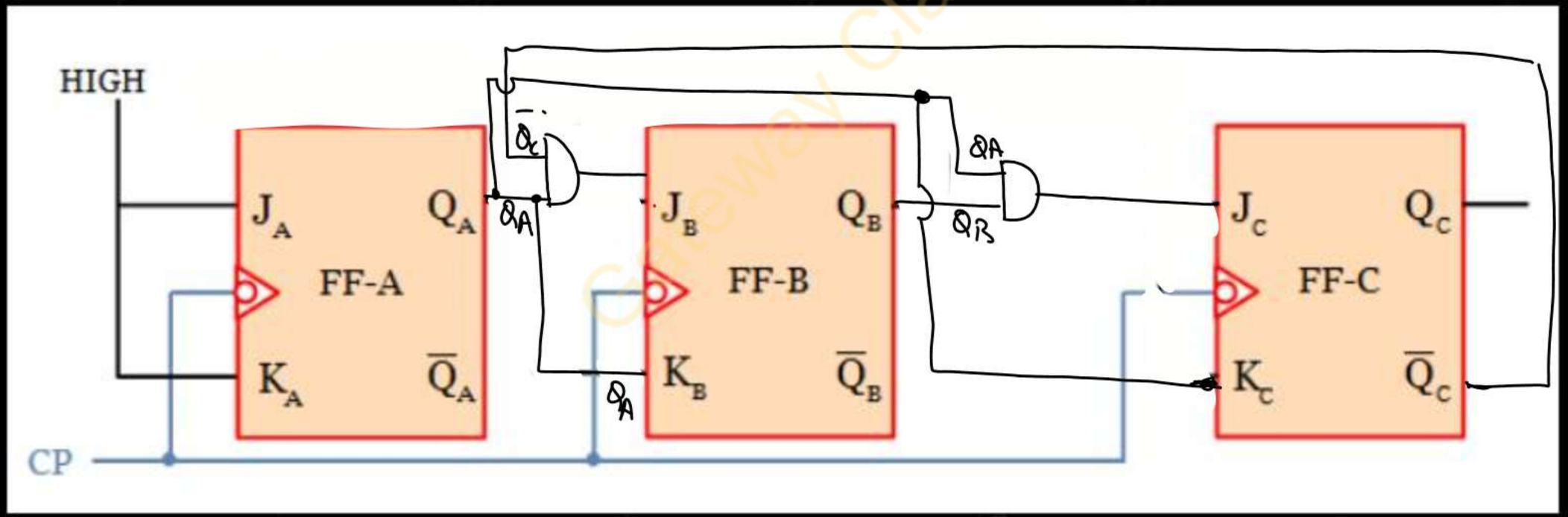
$K_A = 1$

Gateway Classes

Step 6: Draw the logic diagram of the counter.

$J_A = K_A = 1$, $J_B = Q_A \bar{Q}_C$, $K_B = Q_A$, $J_C = Q_A Q_B$, $K_C = Q_A$

MOD- 6 Counter



Gateway Classes

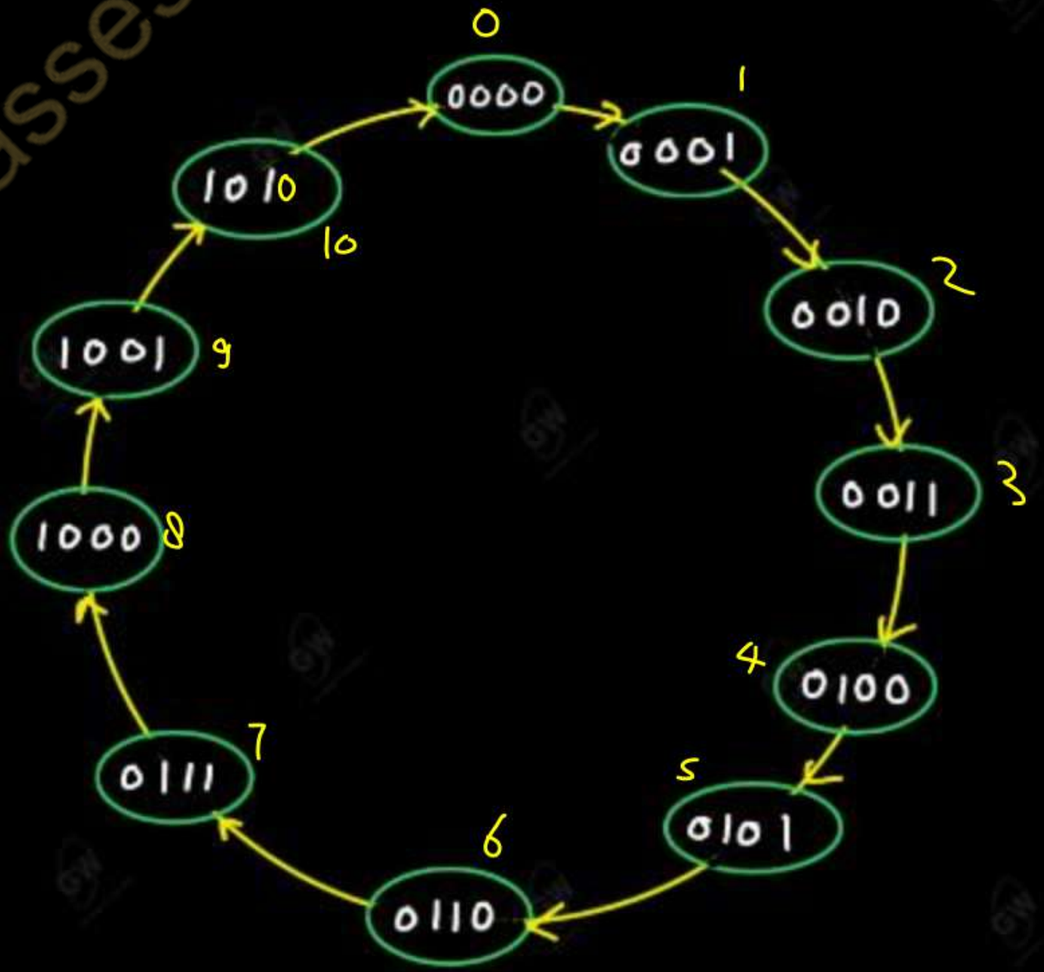
Ex. Design a MOD-11 Counter Using T FF.

AKTU-2021-22

Mod-6 counter represents that the counter will have 11 states (0001 to 1010). Thus, N = 11. That is the number of flip-flops, n = 4.

The state diagram for the mod-6 counter with 11 states is drawn as below.

The excitation table for T flip flop is given by,



Gateway Classes

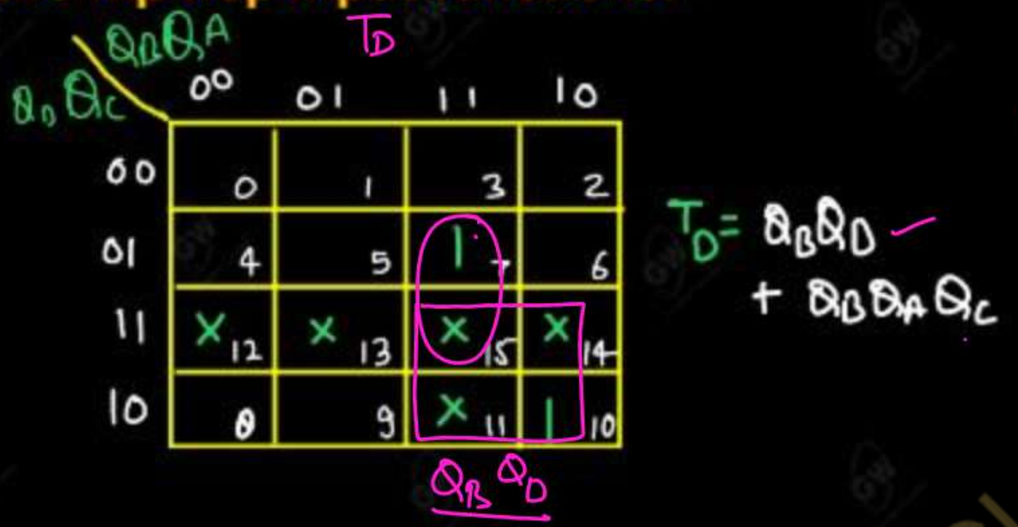
Excitation table for MOD-11 counter

	Present state				Next state				Inputs.				
CLK	Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_D	T_C	T_B	T_A	
1	0	0	0	0	0	0	0	1	0	0	0	1	0
2	0	0	0	1	0	0	1	0	0	0	1	1	1
3	0	0	1	0	0	0	1	1	0	0	0	1	2
4	0	0	1	1	0	1	0	0	0	1	1	1	3
5	0	1	0	0	0	1	0	1	0	0	0	1	4
6	0	1	0	1	0	1	1	0	0	0	1	1	5
7	0	1	1	0	0	1	1	1	0	0	0	1	6
8	0	1	1	1	1	0	0	0	1	1	1	1	7
9	1	0	0	0	1	0	0	1	0	0	0	1	8
10	1	0	0	1	1	0	1	0	0	0	1	1	9
11	1	0	1	0	0	0	0	0	1	0	1	0	10
12	1	0	1	1	x	x	x	x	x	x	x	x	11
13	1	1	0	0	x	x	x	x	x	x	x	x	12
14	1	1	0	1	x	x	x	x	x	x	x	x	13
15	1	1	1	0	x	x	x	x	x	x	x	x	14
16	1	1	1	1	x	x	x	x	x	x	x	x	15

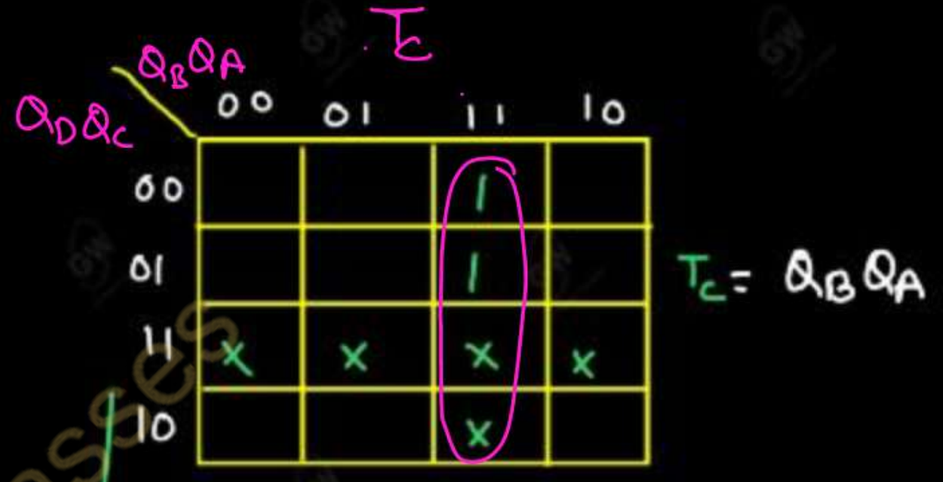
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Gateway Classes

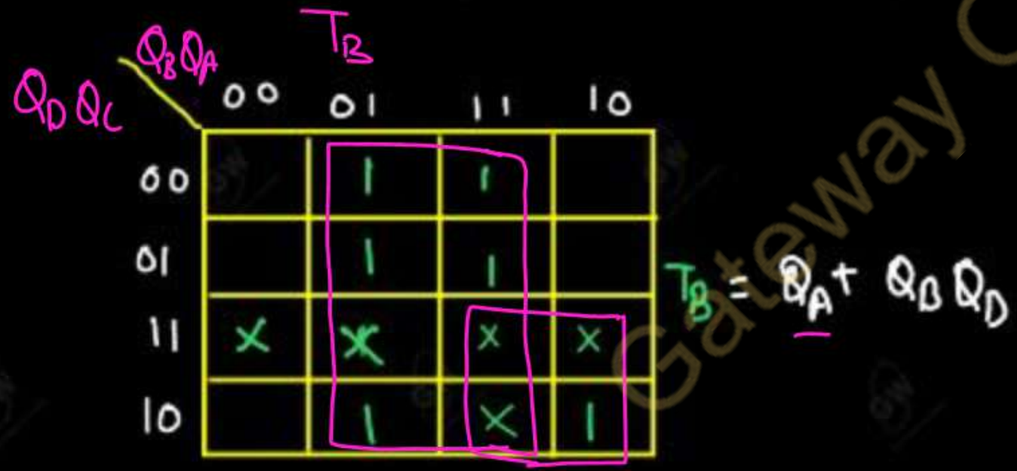
Derive the flip flop input functions.



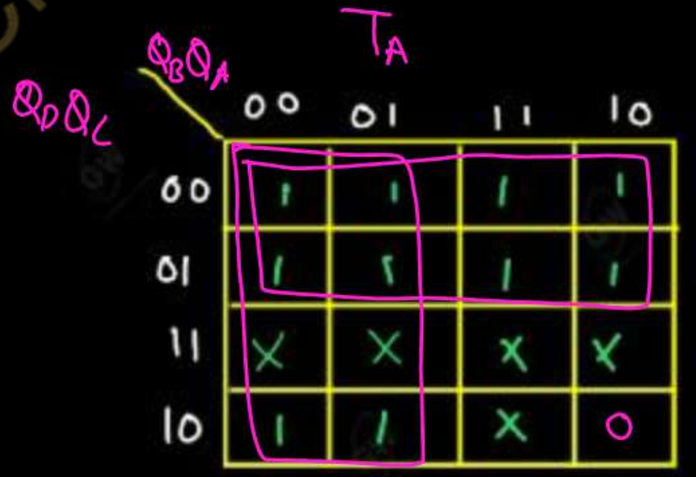
$T_D = Q_B Q_D + Q_B Q_A Q_C$



$T_C = Q_B Q_A$



$T_B = Q_A + Q_B Q_D$



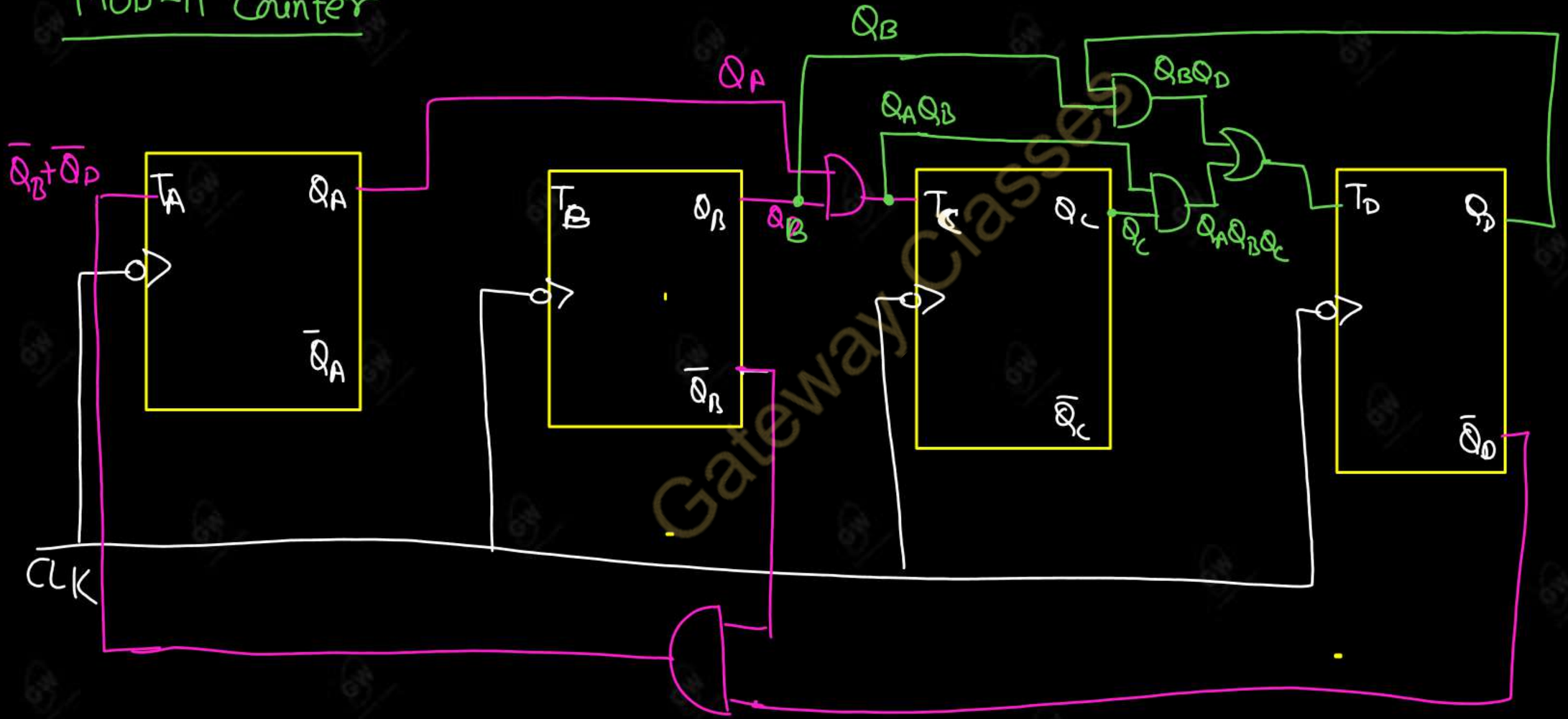
$T_A = \overline{Q_D} + \overline{Q_B}$

Gateway Classes

Logic diagram of the counter.

$T_D = Q_B Q_D + Q_A Q_B Q_C$, $T_C = Q_A Q_B$, $T_B = Q_A + Q_B Q_D$, $T_A = \overline{Q}_B + \overline{Q}_D$

MOD-11 Counter

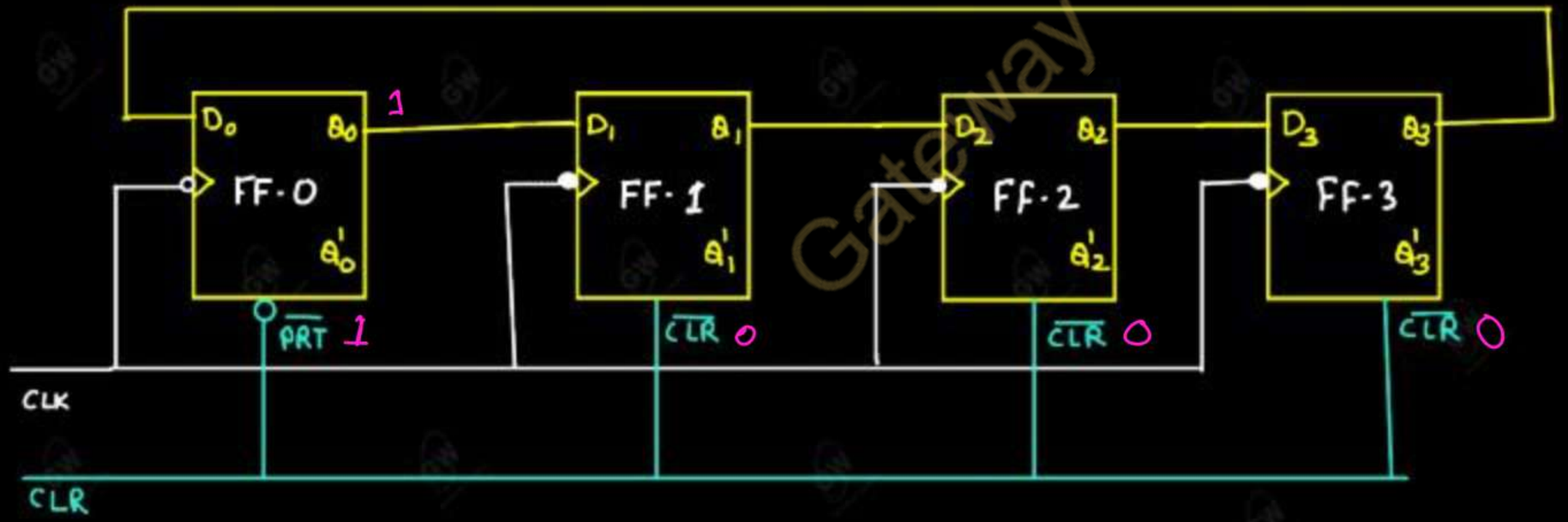


Gateway Classes

Ring counter:

The ring counter is a application of shift register, in which the output of last flip flop is connected to input of first flip flop. In ring counter if the output of any flip flop is 1, then the output of remaining flip flops is 0. The Ring counters transfers the same output throughout the circuit. in a four-register counter, with initial register values of 0000, the repeating pattern is 1000 → 0100 → 0010 → 0001 → 1000.

No of State = 4 , MOD-4



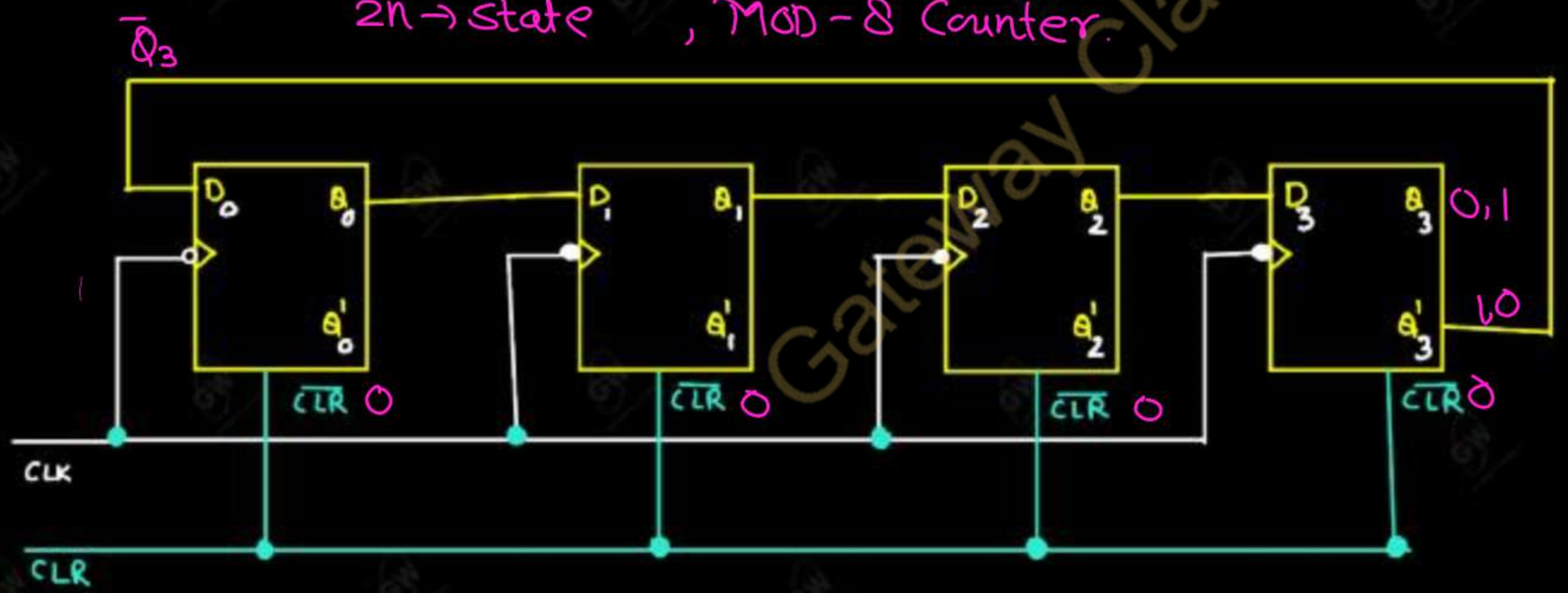
CLK	Q_3	Q_2	Q_1	Q_0	
1	0	0	0	1	1
2	0	0	1	0	2
3	0	1	0	0	4
4	1	0	0	0	8
	0	0	0	1	

Gateway Classes

Johnson's counter or twisted ring counter:

AKTU-2024-25

The Johnson counter is a modification of ring counter. In this the inverted output of the last stage flip flop is connected to the input of first flip flop. If we use n flip flops to design the Johnson counter, it is known as 2n bit Johnson counter or Mod 2n Johnson counter. The Johnson counter circulates a stream of ones followed by zeroes around the ring. For example, in a four-register counter, with initial register values of 0000, the repeating pattern is: 0000, 1000. 1100, 1110, 1111, 0111, 0011, 0001, 0000...

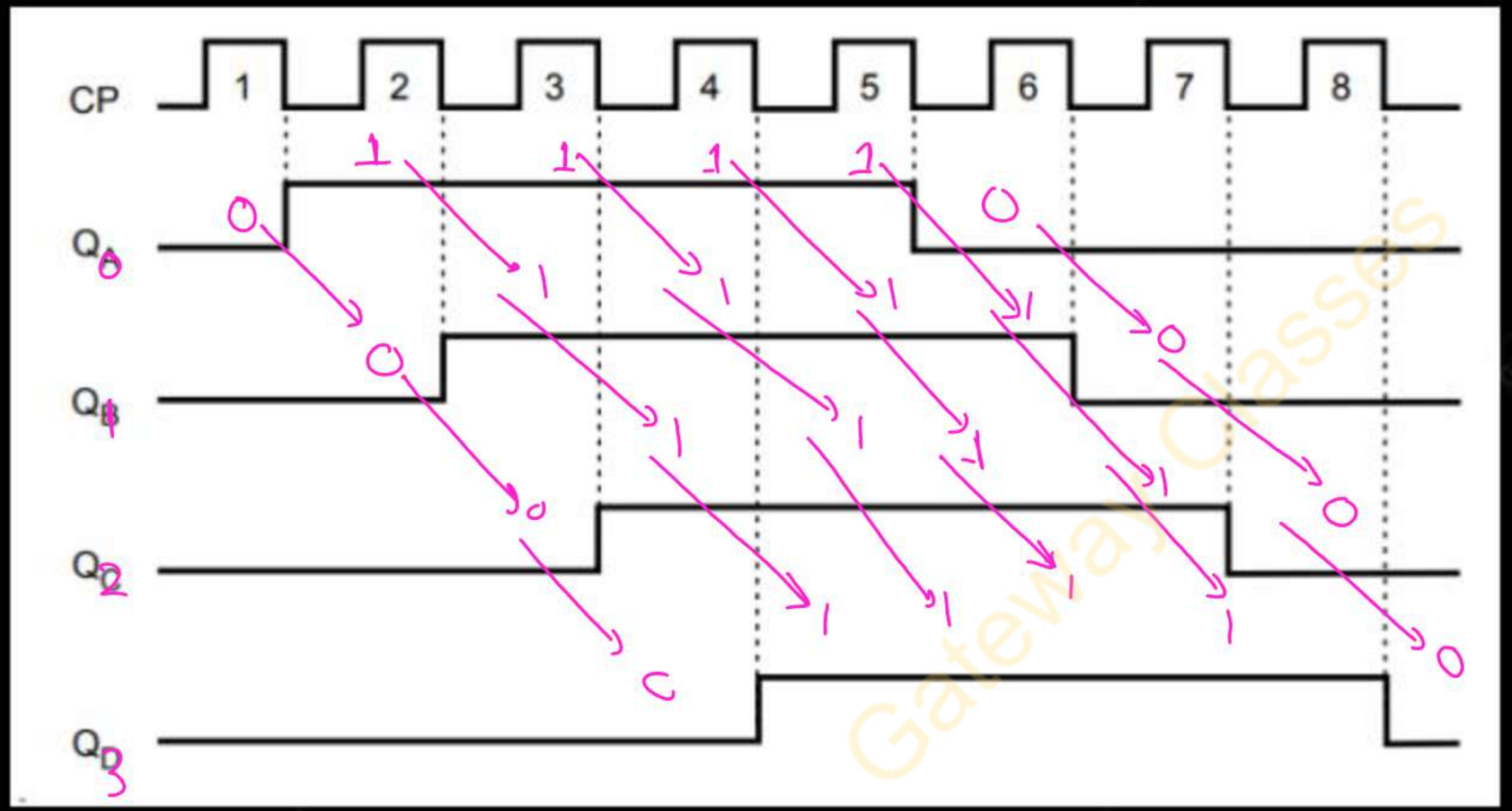


CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1
5	1	1	1	0
6	1	1	0	0
7	1	0	0	0

Gateway Classes

Johnson's counter or twisted ring counter:

AKTU-2024-25



Mod - 2n Counter

No. of flip flop = n

No. of state = 2n

Gateway Classes

AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design



Avinash Sir

Unit-3 Lec-6

Today's target

- Mealy and Moore machines,
- State diagrams, state reduction,
- Analysis of clocked sequential circuits,
- Design of clocked sequential circuits.
- PYQ

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

State & State Variable:- State is defined by the output of Flip flop(Memory). And State Variables are the physical memory elements used in digital hardware to encode and store the current state of the FSM.

State and State Variables are related by the expression.

$$2^x = y$$

$2^2 = 4$



Where x= No. of Flip Flop (Memory) and Y is the Maximum number of possible state.



State Diagram :- A State Diagram is the graphical, visual representation of an FSM's behavior.

Nodes (Circles): Represent the states of the machine.

Arcs (Directed Edges/Arrows): Represent the transitions (movement) from one state to the next.

Labels: ***Mealy Machine:*** Labels on the arcs are in the format Input / Output (e.g., 1/0).

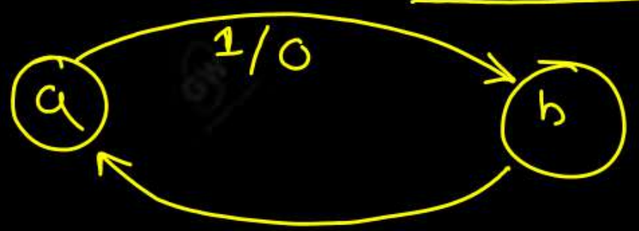
Moore Machine: Labels on the nodes are in the format State Name / Output (e.g., State A / 0), and the arcs are labeled only with the Input.

Starting State: Usually indicated by an arrow pointing into the node from nowhere.

Gateway Classes

Finite State Machine (FSM)

A synchronous sequential circuit is also called as Finite State Machine FSM, if it has a finite number of states.



Components of a Finite State Machine

- **Finite States:-** The finite states are nothing but the distinct modes or conditions in the given system. Each finite states represents a specific behavior. They are represented by symbols or labels.
- **State Transitions:-** It is the change from one state to another. These are generally triggered by events which are associated with some rules or conditions and determine the next state of the system.
- **State Diagram:-** Behavior of a finite state machine can be represented in a graphical form known as state diagrams.
- **Inputs:** They trigger the state transitions in the system.
- **Outputs:-** The results produced by the system are known as outputs.

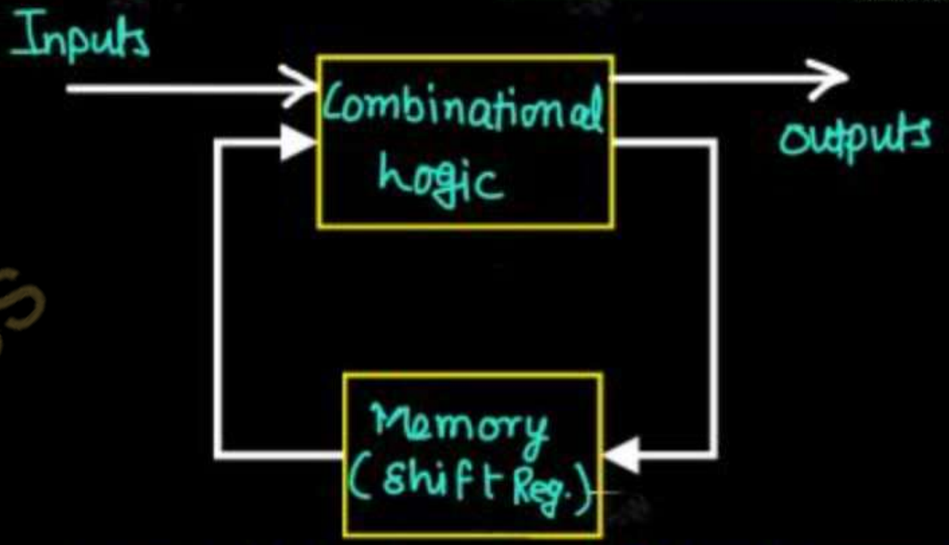
Gateway Classes

GW GATEWAY CLASSES

AKTU-2021-22

FSMs are used in many digital system designs:

- Control units in microprocessors
- Traffic light controllers, Vending machines
- Sequence detectors
- Communication protocols (UART, I2C, etc.)
- Robotics and automation systems



Finite State Machine (FSM) Block Diagram

Advantages of FSM

- Easy to design and analyze.
- Reduces complexity in sequential circuit design.
- Provides a systematic way to represent control logic.
- Useful for both hardware and software implementations.

Limitations of FSM

- Becomes complex for large systems (many states).
- Requires careful state reduction and minimization. Memory usage increases with number of states.

Gateway Classes

Types of FSM

There are two main types of FSMs based on how the outputs depend on states and inputs:

Type	Output Depends On	Diagram Representation	Example
Moore Machine	Current State only	Output shown inside state circle	Sequence detector
Mealy Machine	Current State + Input	Output shown on transition line	Serial data detector

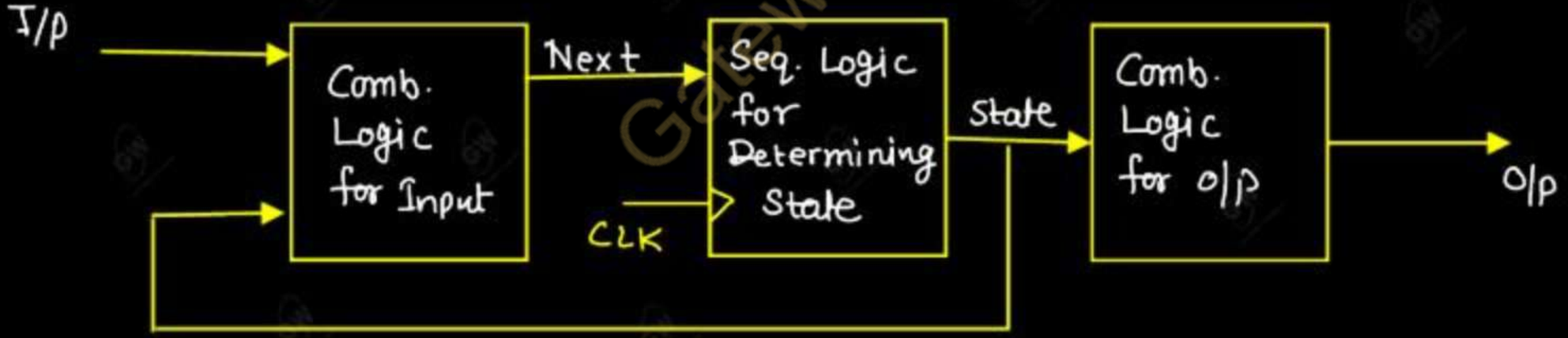
Gateway Classes

Moore Machine

AKTU-2021-22

A Finite State Machine is said to be a Moore state machine, if its *outputs depend only on the present states*. There are two parts presents in a Moore state machine. Those are combinational logic and memory. In this case, the present inputs and present states determine the next states. So, based on next states, Moore machine produces the outputs. So, the outputs will be valid only after transition of the state.

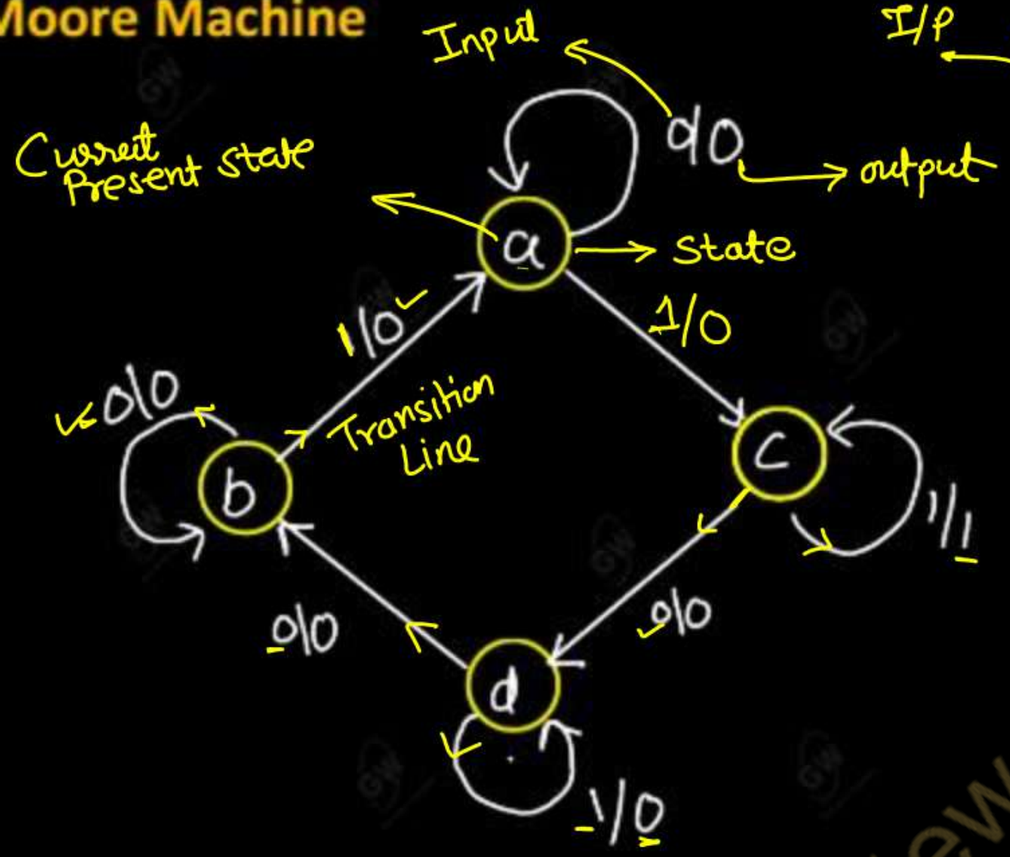
There are four states, namely A, B, C, and D. These states and the respective outputs are labelled inside the circles. Here, only the input value is labeled on each transition.



Gateway Classes

Moore Machine

AKTU-2021-22



I/P — 0 / 1 → o/p

Transition Table

Present state	Next state		output	
	x = 0	x = 1	x = 0	x = 1
a	a	c	0	0
b	b	a	0	0
c	d	c	0	1
d	b	d	0	0

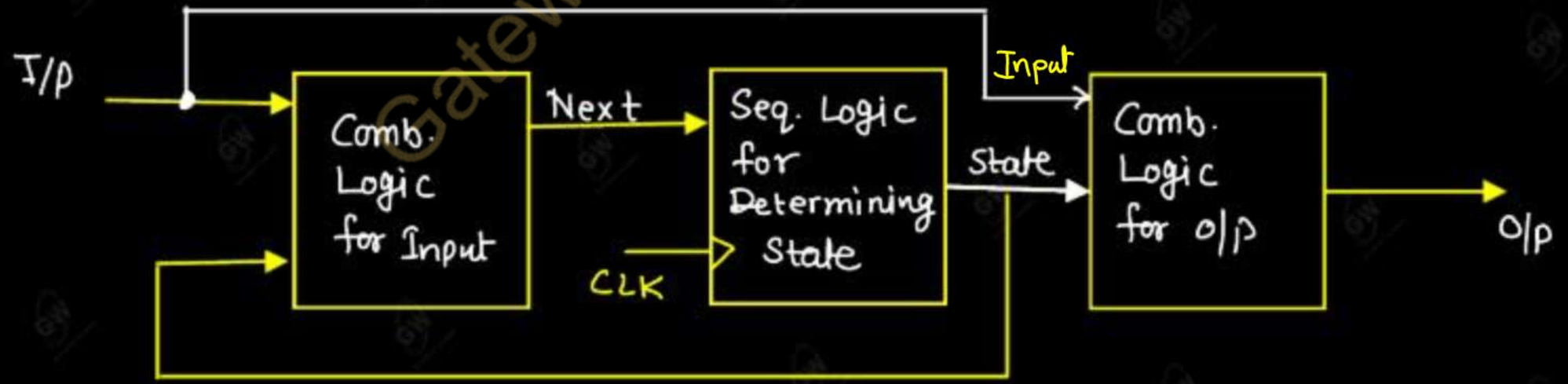
Gateway Classes

Mealy Machine

AKTU-2021-22

In a Mealy state machine, outputs *depend on both present inputs & present states.* There are two main parts presents in the Mealy state machine. Those are combinational logic circuit and memory element. The memory element is useful to provide some part of previous outputs and present states as inputs to the combinational logic circuit.

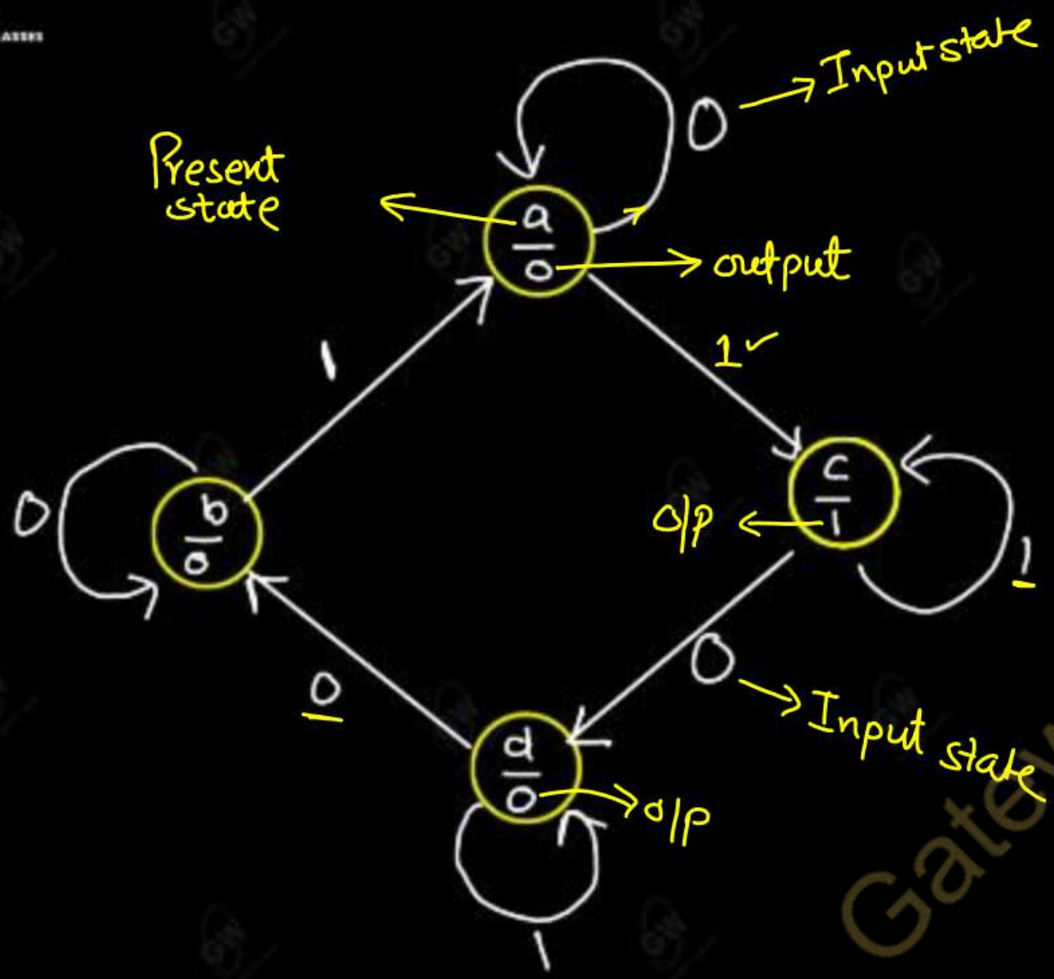
There are three states, namely A, B and C . Each state labelled inside the circles and each circle corresponds to one state. State transitions between these states are represented with directed lines. Here, 0 / 0, 1 / 0 and 1 / 1 denote the input / output. In the above figure, there are two state transitions from each state based on the value of input.



Gateway Classes

Mealy Machine

AKTU-2021-22



Transition Table

Present state	Next state		Output
	x = 0	x = 1	
a	a	c	0
b	b	a	0
c	d	c	1
d	b	d	0

Gateway Classes

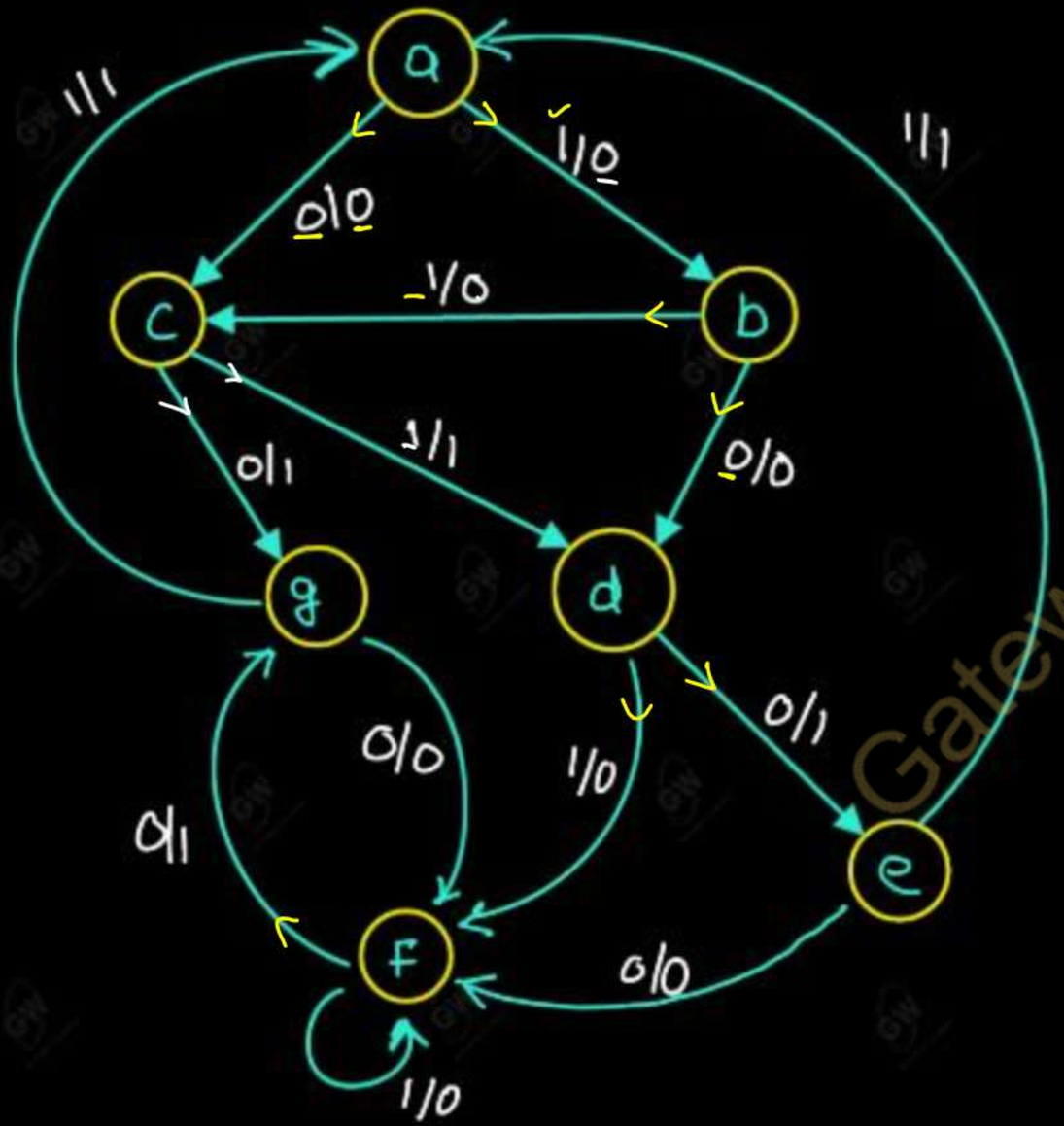
AKTU-2023-24

Difference Between Mealy Machine and Moore Machine

Feature	Mealy Machine	Moore Machine
Output Dependency	Current state and current input	Current state only
Output Timing	Can change during a state transition, based on the input	Changes only when the state changes, synchronized with the clock
Reaction Speed	Faster response to input changes	Slower response, with a one-clock-cycle delay
Number of States	Usually requires fewer states for the same function	Usually requires more states
Design Complexity	Can be more complex to design	Is generally simpler to design
Hardware Requirement	Requires less hardware	Requires more hardware
Output Association	Outputs are associated with the transitions between states	Outputs are associated with the states themselves

Gateway Classes

State Diagram and State Reduction



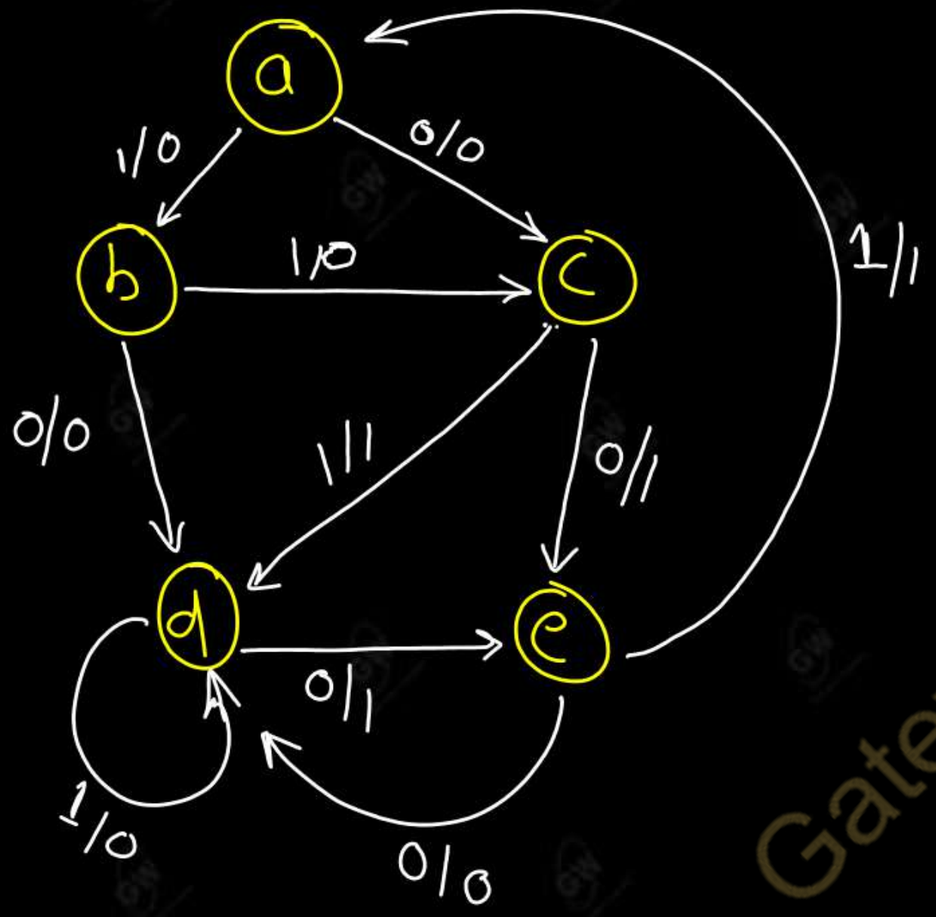
Transition Table

Present State	Next State		output	
	$x=0$	$x=1$	$x=0$	$x=1$
a	c	b	0	0
b	d	c	0	0
c	g(e)	d	1	1
d	e(g)	f(d)	1	0
e	f(d)	a	0	1
→ f	g	f	1	0
→ g	f	a	0	1

$e = g$, $f = d$

Gateway Classes

State Diagram and State Reduction



Reduced transition Table.

Present State	Next State		output	
	$x=0$	$x=1$	$x=0$	$x=1$
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	d	1	0
e	d	a	0	1

Gateway Classes

State Assignment

Present State	Next State		output	
	$x=0$	$x=1$	$x=0$	$x=1$
000	010	001	0	0
001	011	010	0	0
010	100	011	1	1
011	100	011	1	0
100	011	000	0	1

hot

a = 000 , b = 001 , c = 010

d = 011 , e = 100

No. of bit = 2

$2^2 = 4$

No. of bit = 3

$2^3 = 8$

Gateway Classes

Design Procedure of Circuit

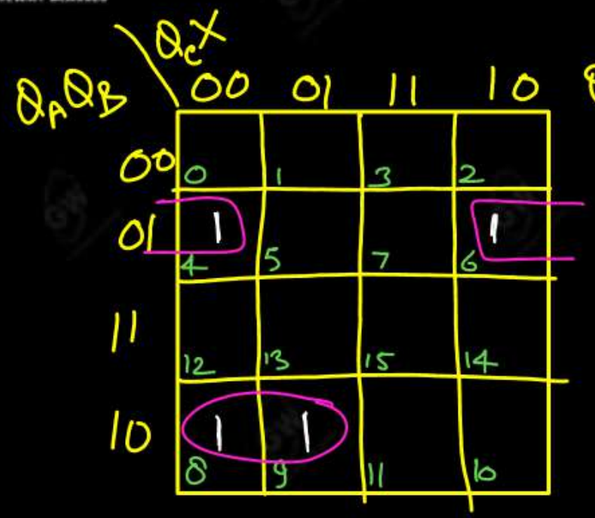
	Present state			Input	Next state			Inputs of flip flop		
	Q_A	Q_B	Q_C	x	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1	0
1	0	0	0	1	0	0	1	0	0	1
2	0	0	1	0	0	1	1	0	1	0
3	0	0	1	1	0	1	0	0	1	1
4	0	1	0	0	1	0	0	1	1	0
5	0	1	0	1	0	1	1	0	0	1
6	0	1	1	0	1	0	0	1	1	1
7	0	1	1	1	0	1	1	0	0	0
8	1	0	0	0	0	1	1	1	1	1
9	1	0	0	1	0	0	0	1	0	0

Excitation Table

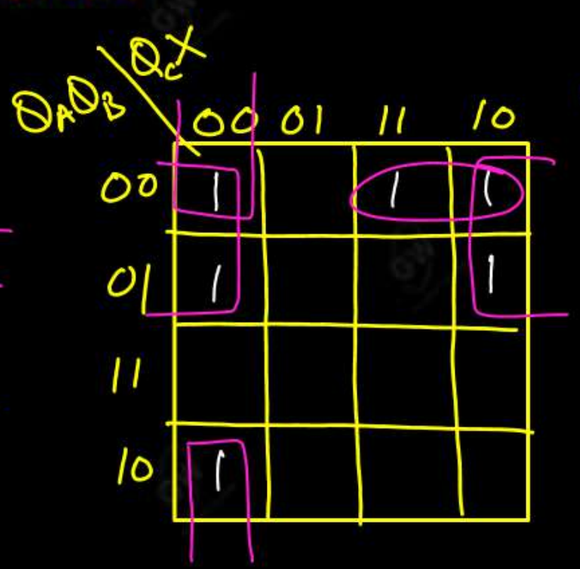
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Gateway Classes

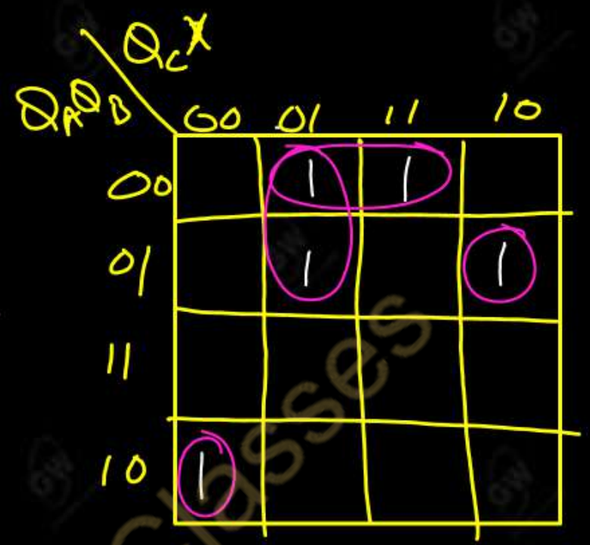
Design Procedure of Circuit



$$T_A = Q_A\bar{Q}_B\bar{Q}_C + \bar{Q}_AQ_B\bar{X}$$



$$T_B = \bar{Q}_A\bar{X} + \bar{Q}_A\bar{Q}_BQ_C + \bar{Q}_B\bar{Q}_C\bar{X}$$



$$T_C = \bar{Q}_A\bar{Q}_BX + \bar{Q}_A\bar{Q}_CX + \bar{Q}_AQ_BQ_C\bar{X} + Q_A\bar{Q}_B\bar{Q}_C\bar{X}$$

Gateway Classes

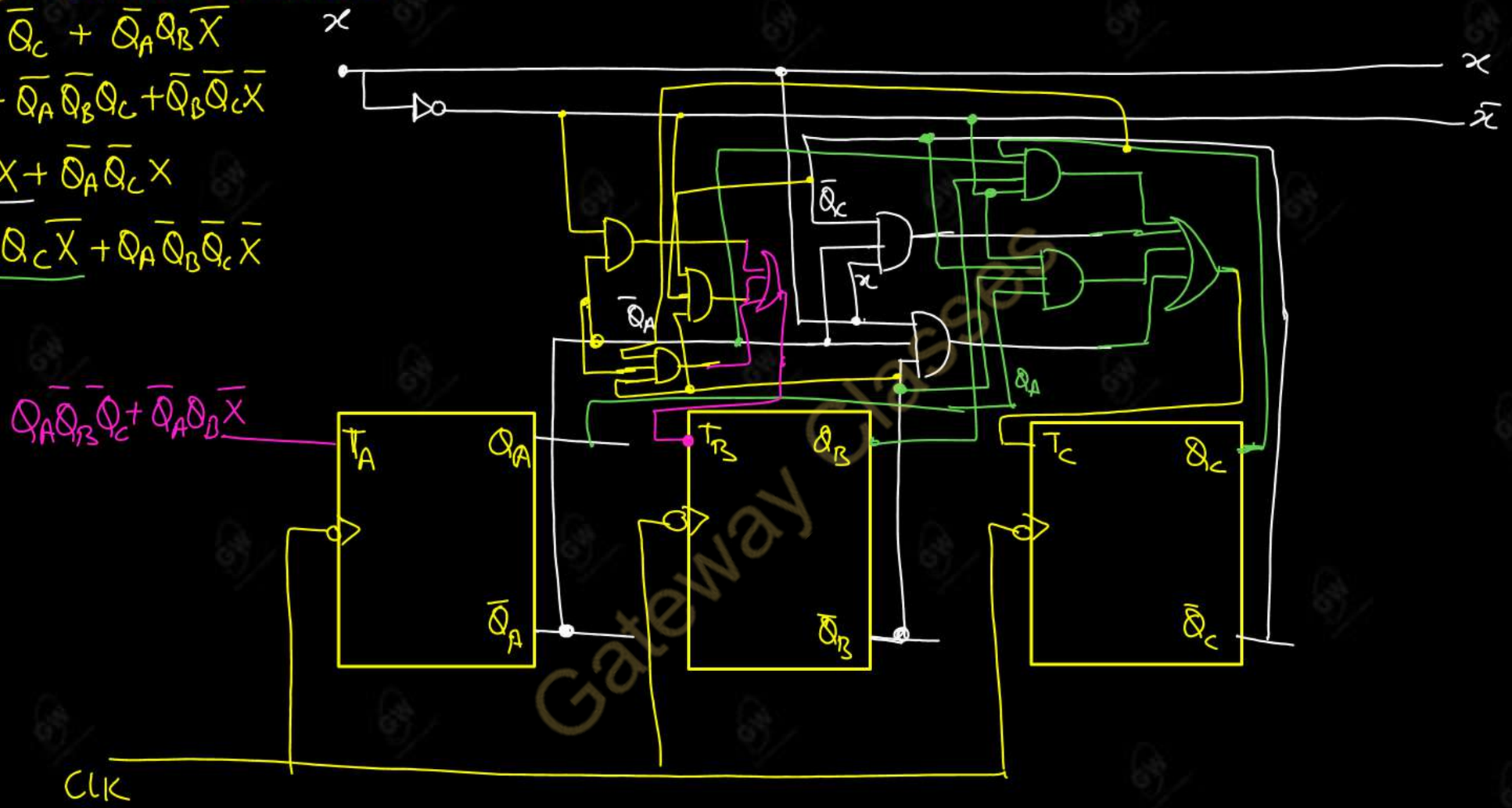
Design Procedure of Circuit

$$T_A = Q_A \bar{Q}_B \bar{Q}_C + \bar{Q}_A Q_B \bar{X}$$

$$T_B = \bar{Q}_A \bar{X} + \bar{Q}_A \bar{Q}_B Q_C + \bar{Q}_B \bar{Q}_C \bar{X}$$

$$T_C = \bar{Q}_A \bar{Q}_B X + \bar{Q}_A \bar{Q}_C X + \bar{Q}_A Q_B Q_C \bar{X} + Q_A \bar{Q}_B \bar{Q}_C \bar{X}$$

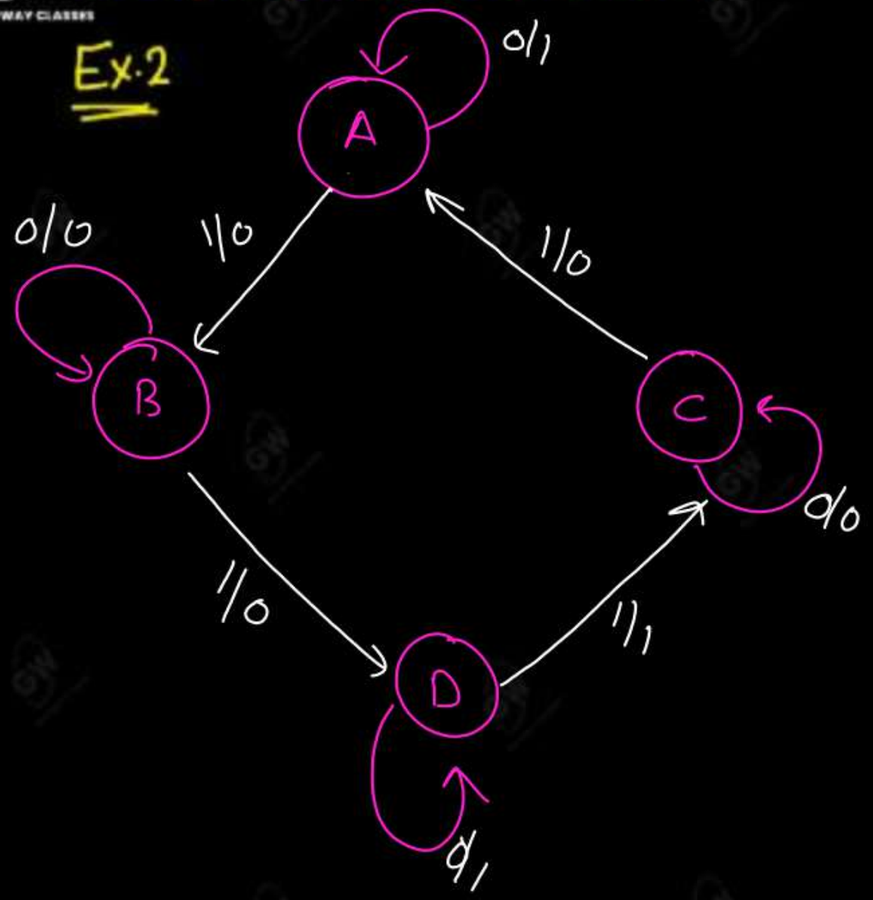
X



Gateway Classes

Design Procedure of Circuit

Ex.2



State table

P.S.	N.S		output	
	x=0	x=1	x=0	x=1
A	A	B	1	0
B	B	D	0	0
C	C	A	0	0
D	D	C	1	1

④ state

$2^n = 4$

$n = 2$

let A = 00
B = 01
C = 10
D = 11

Gateway Classes

Design Procedure of Circuit

J-K

Ex.2

	P.S		I/P	Next state		I/P for ff			
	Q_A	Q_B	X	Q_{A+1}	Q_{B+1}	J_A	K_A	J_B	K_B
A	0	0	0	0	0 0	0	X	0	X
	0	0	1	0	1 1	0	X	1	X
B	0	1	0	0	1 2	0	X	X	0
	0	1	1	1	1 3	1	X	X	0
C	1	0	0	1	0 4	X	0	0	X
	1	0	1	0	0 5	X	1	0	X
D	1	1	0	1	1 6	X	0	X	0
	1	1	1	1	0 7	X	0	X	1

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J_A

Q_A \ Q_BX	00	01	11	10
0			1	
1	X	X	X	X

$J_A = Q_B\bar{X}$

K_A

Q_A \ Q_BX	00	01	11	10
0	X 0	1 1	X 3	X 2
1	1 4	5	7	6

$K_A = \bar{Q}_B X$

J_B

Q_A \ Q_BX	00	01	11	10
0		1	X	X
1			X	X

$J_B = \bar{Q}_A X$

K_B

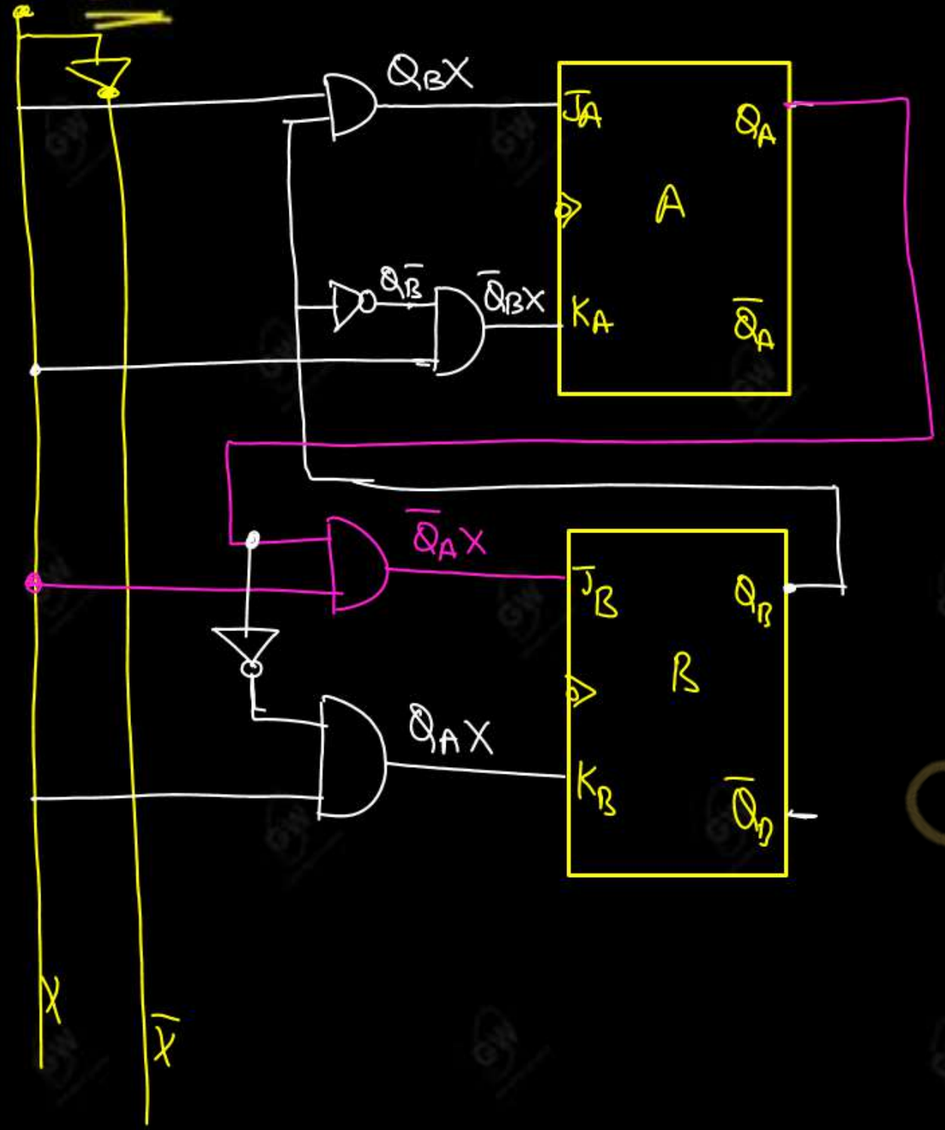
Q_A \ Q_BX	00	01	11	10
0	X	X		
1	X	X	1	

$K_B = Q_A X$

Gateway Classes

Design Procedure of Circuit

Ex.2



$J_A = Q_B X$

$K_A = \bar{Q}_B X$

$J_B = \bar{Q}_A X$

$K_B = Q_A X$

Gateway Classes

Analysis of Clocked Sequential Circuits

The analysis of sequential circuit consists of obtaining a table or a diagram for the time sequence of inputs, outputs and internal states.

Ex 1. Construct the transition table, state table and state diagram for the Moore sequential circuit

1. Determine the flip-flop input equations and the output equations from the sequential circuit.

$$Z = xQ$$

$$T = xQ + \bar{x}\bar{Q}$$

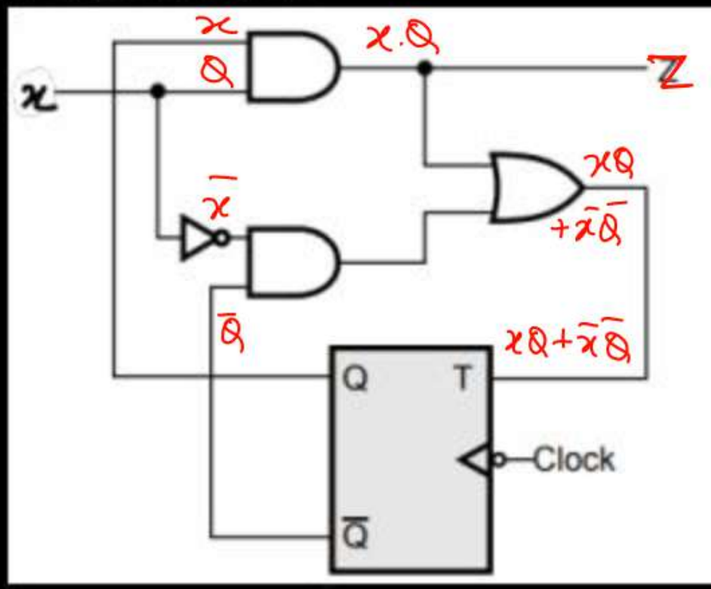
2. Derive the transition equation.

$$Q^+ = T \oplus Q$$

$$Q^+ = (xQ + \bar{x}\bar{Q}) \oplus Q$$

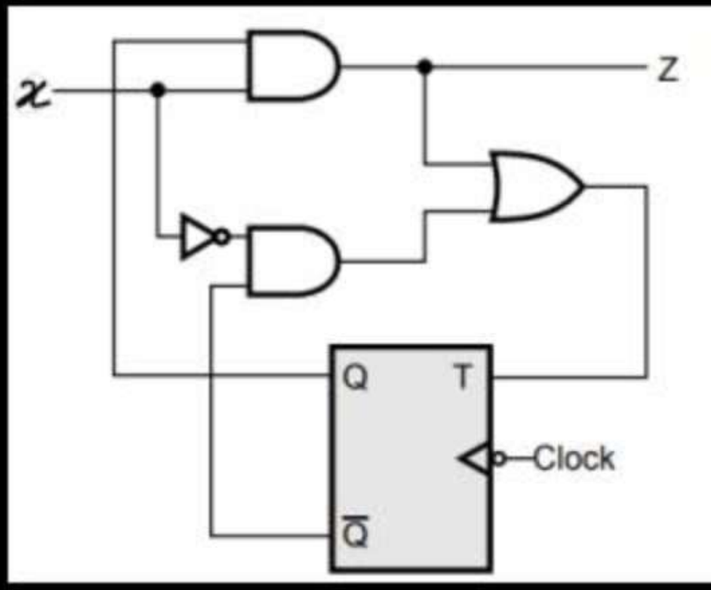
3. Plot the next step map for each flip-flop

$$Q^+ = (xQ + \bar{x}\bar{Q}) \oplus Q$$



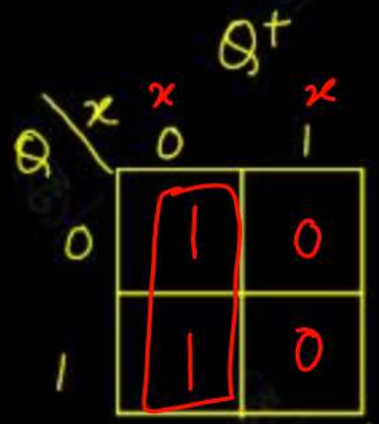
Gateway Classes

Analysis of Clocked Sequential Circuits



4. Plot the transition table

Present state	Next state		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
Q	Q^+	Q^+	Z	Z
$Q=0$	1	0	0	0
$Q=1$	1	0	0	1



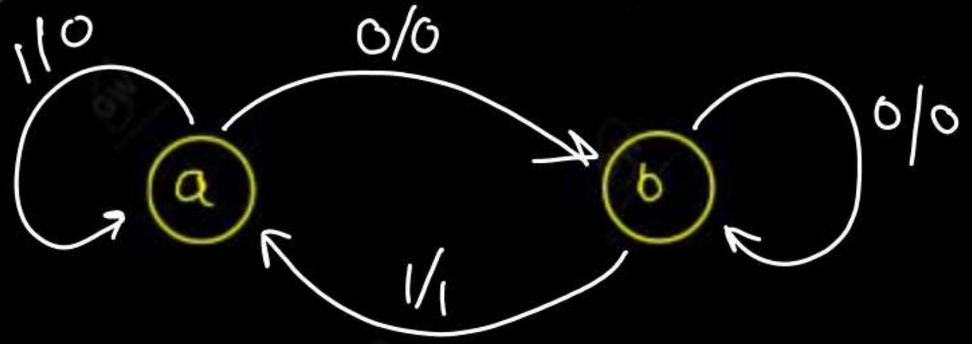
$Q^+ = \bar{x}$

5. Draw the state table $1 \rightarrow b$, $0 \rightarrow a$ $a=0, b=1$

Transition table can be converted into state table. Here, new symbols to binary codes are assigned. a = 0, b = 1.

Present state	Next state		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
a(0)	b	a	0	0
b(1)	b	a	0	1

6. Draw State Diagram



Gateway Classes

Analysis of Clocked Sequential Circuits

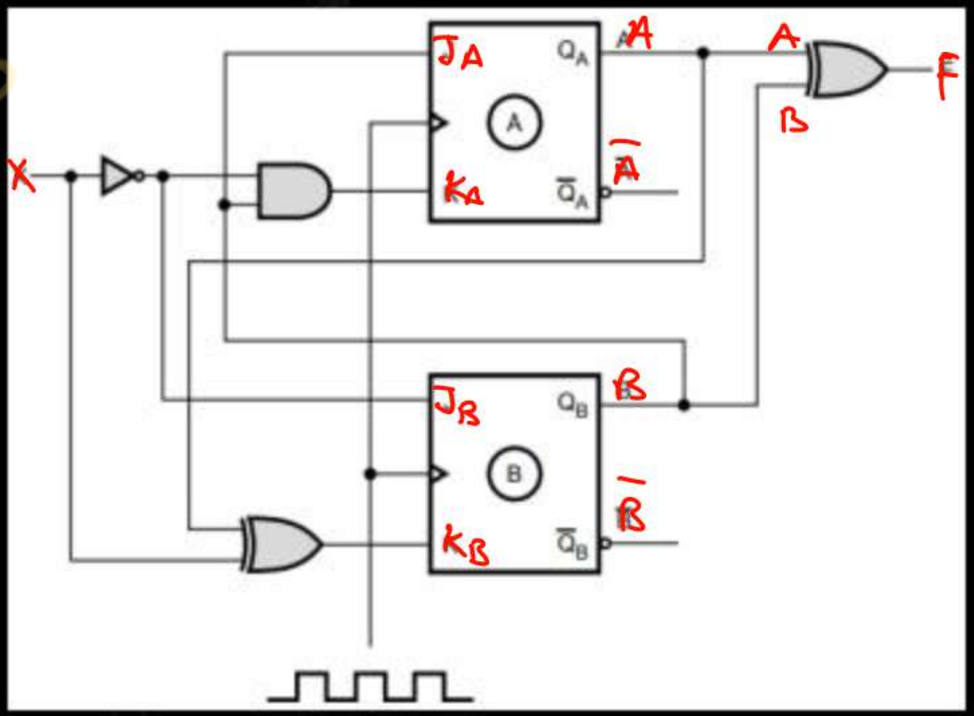
Ex 2. Construct the transition table, state table and state diagram for the Moore sequential circuit

1. Determine the flip-flop input equations and the output equations from the sequential circuit.

$F = A \oplus B$ ✓

$J_A = B$, $K_A = \bar{X}B$

$J_B = \bar{X}$, $K_B = X \oplus A$



2. Derive the transition equation.

$Q^+ = J\bar{Q} + \bar{K}Q$ → G.E.

So $A^+ = Q_A^+ = J_A\bar{Q}_A + \bar{K}_A Q_A = B\bar{Q}_A + \overline{\bar{X}B}Q_A = B\bar{Q}_A + (X+\bar{B})Q_A = B\bar{A} + (X+\bar{B})A$

& $B^+ = Q_B^+ = J_B\bar{Q}_B + \bar{K}_B Q_B = \bar{X}\bar{Q}_B + \overline{(X \oplus A)}\cdot Q_B = \bar{X}\bar{B} + (X \oplus A)\cdot B$

3. Plot the next step map for each flip-flop

For A^+

$B\bar{A} + (X+\bar{B})\bar{A}$

AB \ X	0	1
00		
01	1	1
10	1	1
11		1

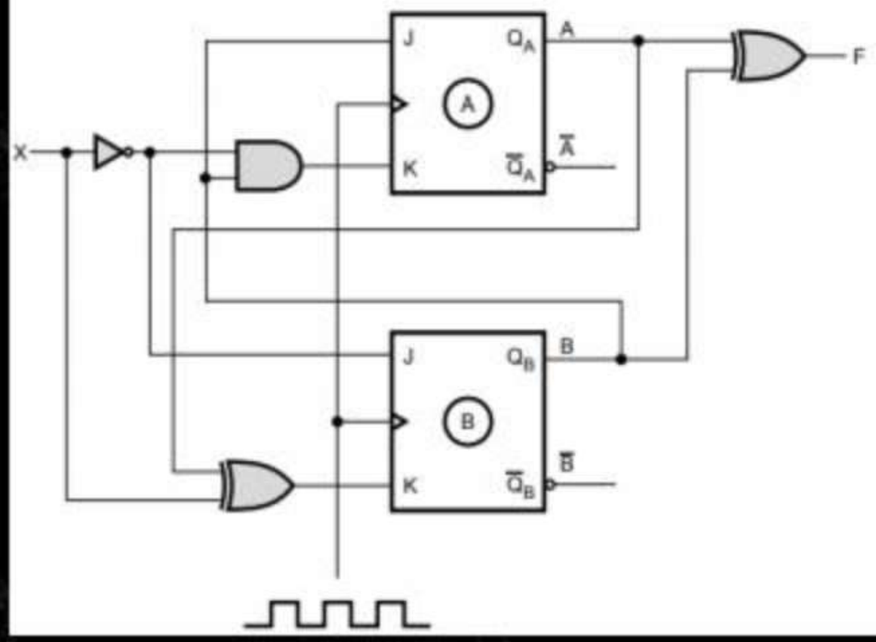
For B^+

AB \ X	0	1
00	1	
01	1	
10	1	
11		1

$\bar{X}\bar{B} + (\overline{X \oplus A})\cdot B$

Gateway Classes

Analysis of Clocked Sequential Circuits



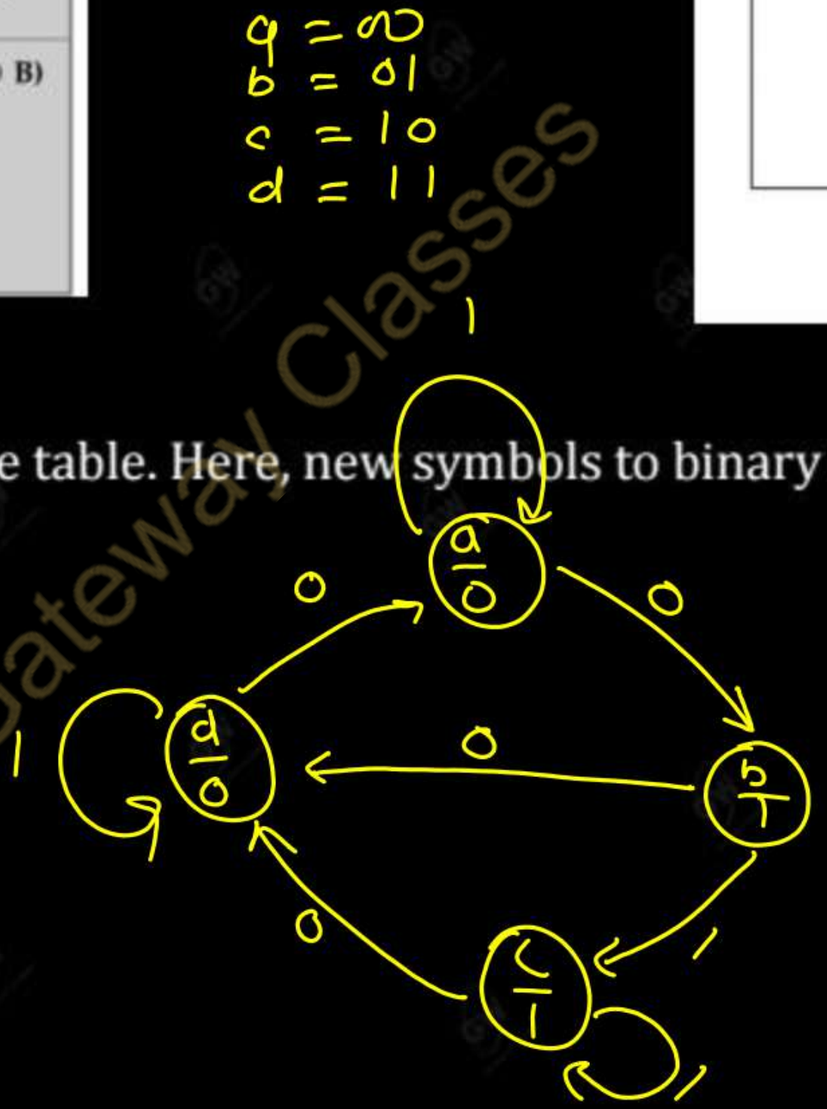
4. Plot the transition table

Present state		Next state				Output
		X = 0		X = 1		
A	B	A^+	B^+	A^+	B^+	F = (A ⊕ B)
0	0	0	1	0	0	0
0	1	1	1	1	0	1
1	0	1	1	1	0	1
1	1	0	0	1	1	0

5. Draw the state table

Transition table can be converted into state table. Here, new symbols to binary codes are assigned

Present state	Next state		Output
A B	X = 0	X = 1	F
	A^+B^+	A^+B^+	
a	b	a	0
b	d	c	1
c	d	c	1
d	a	d	0



In case of Moore model, the directed lines are labelled

Gateway Classes

Gateway Classes

Empowering Learners, Transforming Futures

GATEWAY CLASSES

Thank You

Gateway Classes

GET IT ON Google Play

Download on the App Store

Helpline No- 7819 0058 53