A K T U

B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-4 Lec-2



Avinash Sir

Today's target

- ECL Logic families
- CMOS
- PYQ

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT- 4

- Logic families and semiconductor memories: TTL NAND gate, specifications, noise margin, propagation delay, fan-in, fan-out, tristate TTL, ECL, CMOS families and their interfacing, memory elements, concept of programmable logic devices like FPGA, logic implementation using programmable devices.

Gateway Classes

ECL Logic Families
(unsaturated)

AKTU 2021-22

- The TTL family uses transistors operating in the saturation mode. As a result, their switching speed is limited by the storage delay time associated with a transistor that is driven into saturation.

- Another logic family has been developed that prevents transistor saturation, thereby increasing *overall switching speed* by using a radically different circuits structure, called Current Mode Logic (CML). This logic family is also called Emitter-Coupled Logic (ECL).

- Unlike TTL and CMOS families, ECL does not produce a large voltage swing between the LOW and HIGH levels. It has a small voltage swing, less than a volt, and it internally switches current between two possible paths, depending on the output state.

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Characteristics of a ECL Logic Family

1. **Highest Speed Logic Family :-** ECL is the fastest among all logic families. 10K and 100K ECL have propagation delays around 1 ns. Newer versions like ECL-in-PS achieve delays below 0.5 ns (500 ps).

2. **No Transistor Saturation:-** Transistors are deliberately prevented from entering complete saturation, which avoids storage delays and allows very fast switching.

3. **Small Logic Level Swing:-** The voltage difference between logic HIGH and LOW is kept very small. This prevents transistors from saturating when the input goes from LOW to HIGH.

4. **Low Noise Margins**:- Because the logic levels are close together, ECL has poor noise immunity and is more sensitive to noise compared to other logic families.

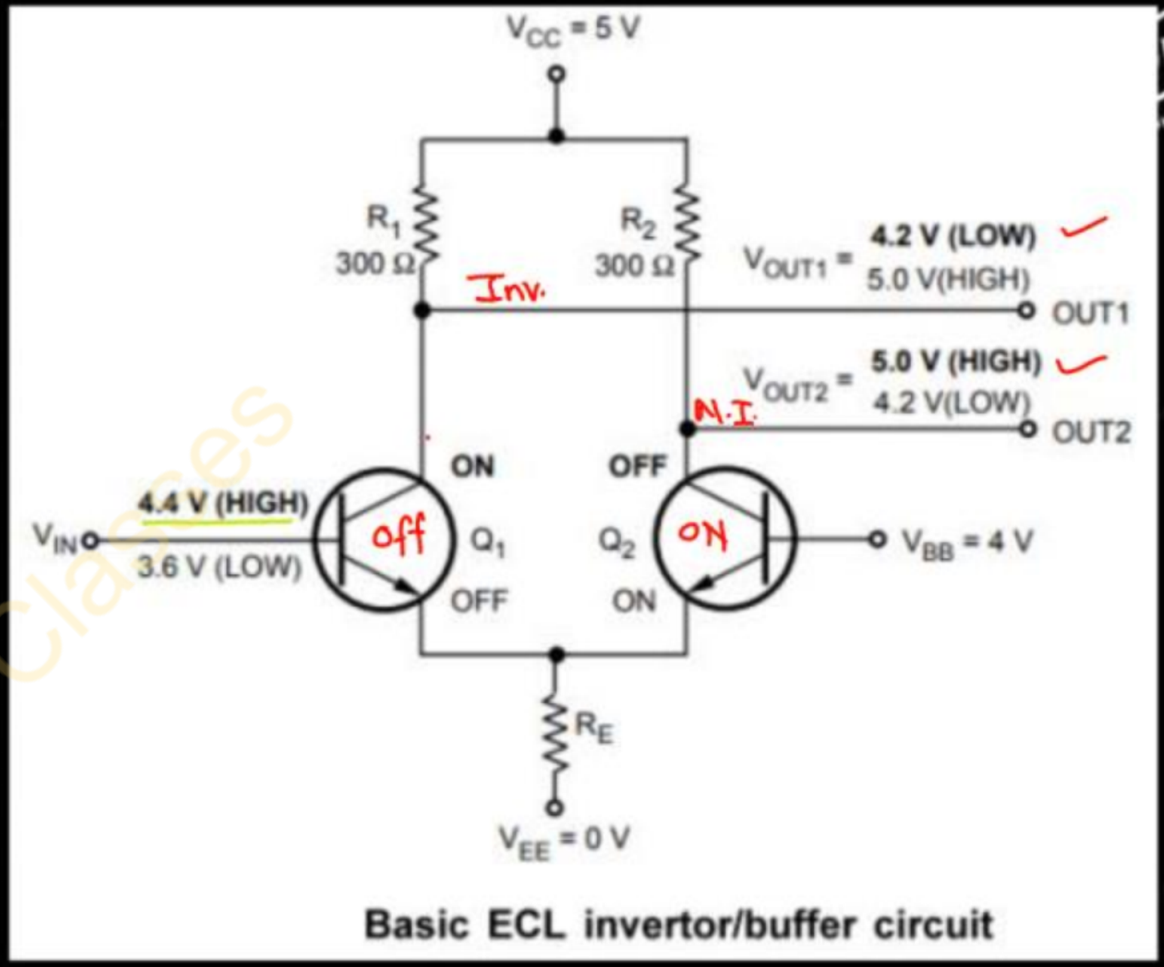
5. **High Power Consumption**:- Since transistors continuously operate in the active region (not saturated), ECL circuits consume more power.

6. **Low Switching Transients:-** The power supply current in ECL remains almost constant, resulting in lower switching noise than TTL or CMOS circuits.

Gateway Classes

Basic ECL Circuit

- It consists of two transistors connected in differential single ended input mode with a common emitter resistance. The circuit has two outputs : inverting output (OUT1) and noninverting output (OUT2). For this circuit, the input LOW and HIGH voltage levels are defined as 3.6 V and 4.4 V, and it produces output LOW and HIGH levels as 4.2 V and 5.0 V.



Basic ECL invertor/buffer circuit

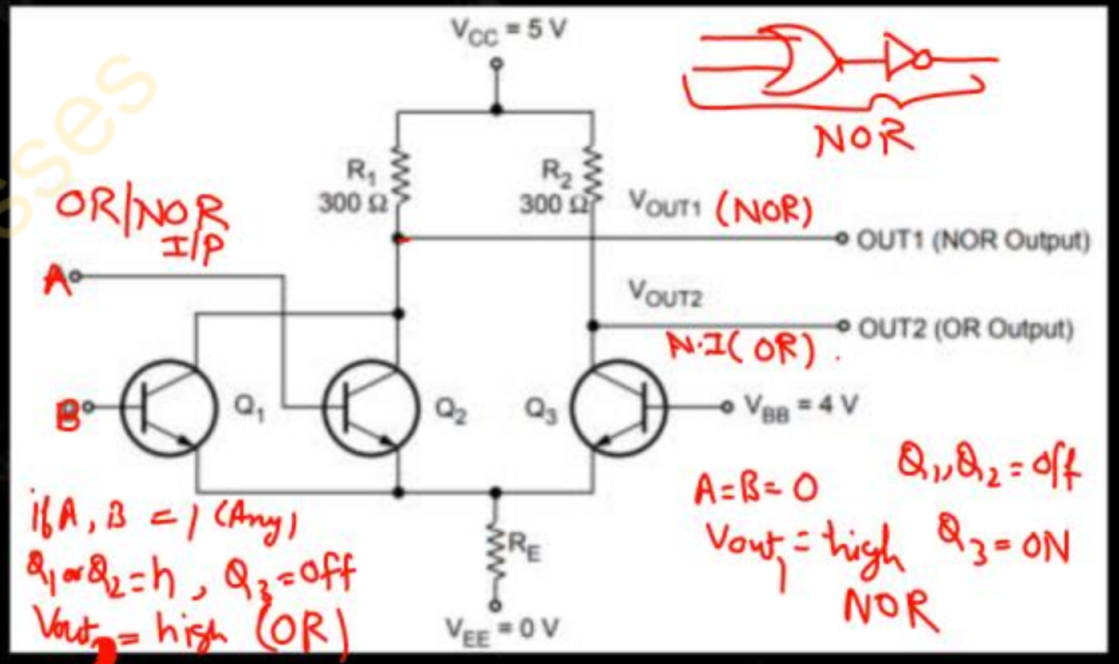
- When V_{IN} is HIGH (4.4 V), (see bold figures) transistor Q_1 is ON, but not saturated and transistor Q_2 is OFF. Thus, V_{OUT2} is pulled to 5.0 V (HIGH) through R_1 and drop across R_2 is 0.8 V so that V_{OUT2} is 4.2 V (LOW).
- When V_{IN} is LOW (3.6 V) (see normal figures), transistor Q_2 is ON, but not saturated and transistor Q1 is OFF. Thus, V_{QUT1} is pulled to 5.0 V (HIGH) through R_1 and drop across R2 is 0.8 V so that V_{OUT2} is 4.2 V (LOW).

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2-Input ECL OR / NOR Gate

There has an additional transistor in parallel with Q1 as compared to ECL inverter. When the inputs applied at both the Q1 & Q2 transistors are low then will make the output1 (Vout1) to a HIGH value. So, this Vout1corresponds to the output of the NOR gate.

- Simultaneously, if the Q3 transistor is turned ON, then it will make the second output (Vout2) to be HIGH. So, this Vou2 output corresponds to the OR gate output.
- In the same way, if both the Q1 &Q2 transistors inputs are HIGH, then it will turn on the Q1 & Q2 transistors and provides the low output at the VOUT1 terminal.
- If the Q3 transistor is turned OFF throughout this operation then it will provide high output at the VOUT2 terminal.



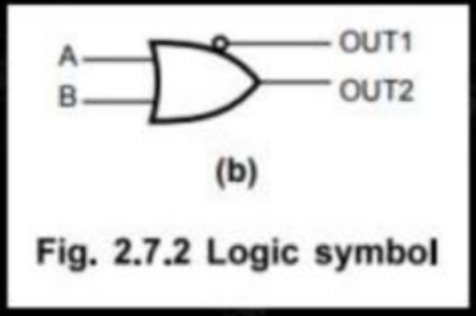


Fig. 2.7.2 Logic symbol

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Advantages and Disadvantages of ECL Family

Advantages of ECL family

1. It is a fastest logic family. Offers propagation delay about 1 ns.
2. Transistors are not allowed to go into complete saturation and thus eliminating storage delays.
3. Less switching transients since power supply current is more stable.
4. Large fan-out.

Disadvantages of ECL family

1. Low noise immunity.
2. High power dissipation.

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