AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-3 Lec-2



Avinash Sir

Today's target

- Types of Flip Flop
- Extinction Table
- PYQ

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

Flip Flops:-

The flip-flop is a circuit that maintains a state until directed by input to change the state. A basic flip-flop can be constructed using four-NAND or four-NOR gates.

A flip-flop is popularly known as the basic digital memory circuit. It has its two states as logic 1(High) and logic 0 (Low) states.

Types of Flip-Flops

- SR Flip Flop
- JK Flip Flop
- D Flip Flop
- T Flip Flop

Gateway Classes

Differences between latches and flip-flops

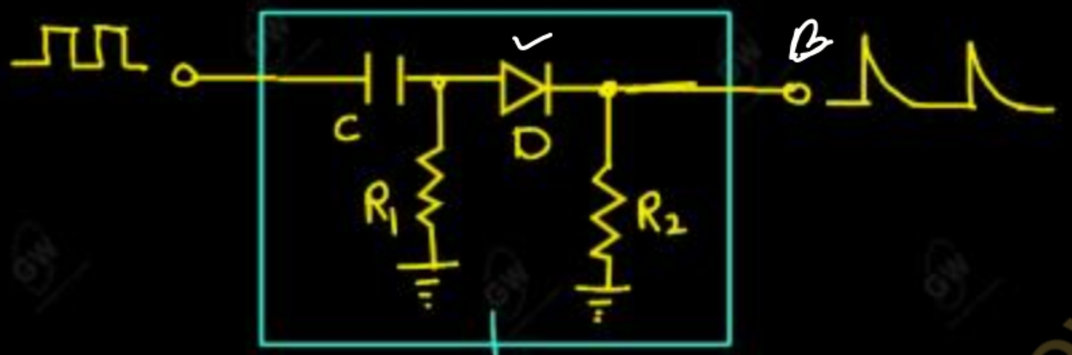
Latches	Flip-flops
Level triggered	Edge triggered
Asynchronous device	Synchronous device
Doesn’t contain clock signal	Contains a clock signal
It will change its state as long as it is enabled	It will change its state only during a given clock cycle
Consumes less power	Consumes more power
Faster	Slower
Examples: D-Latch, T-Latch	Examples: D-Flip flop, T-Flop flop

Gateway Classes

Edge Triggered Flip Flops

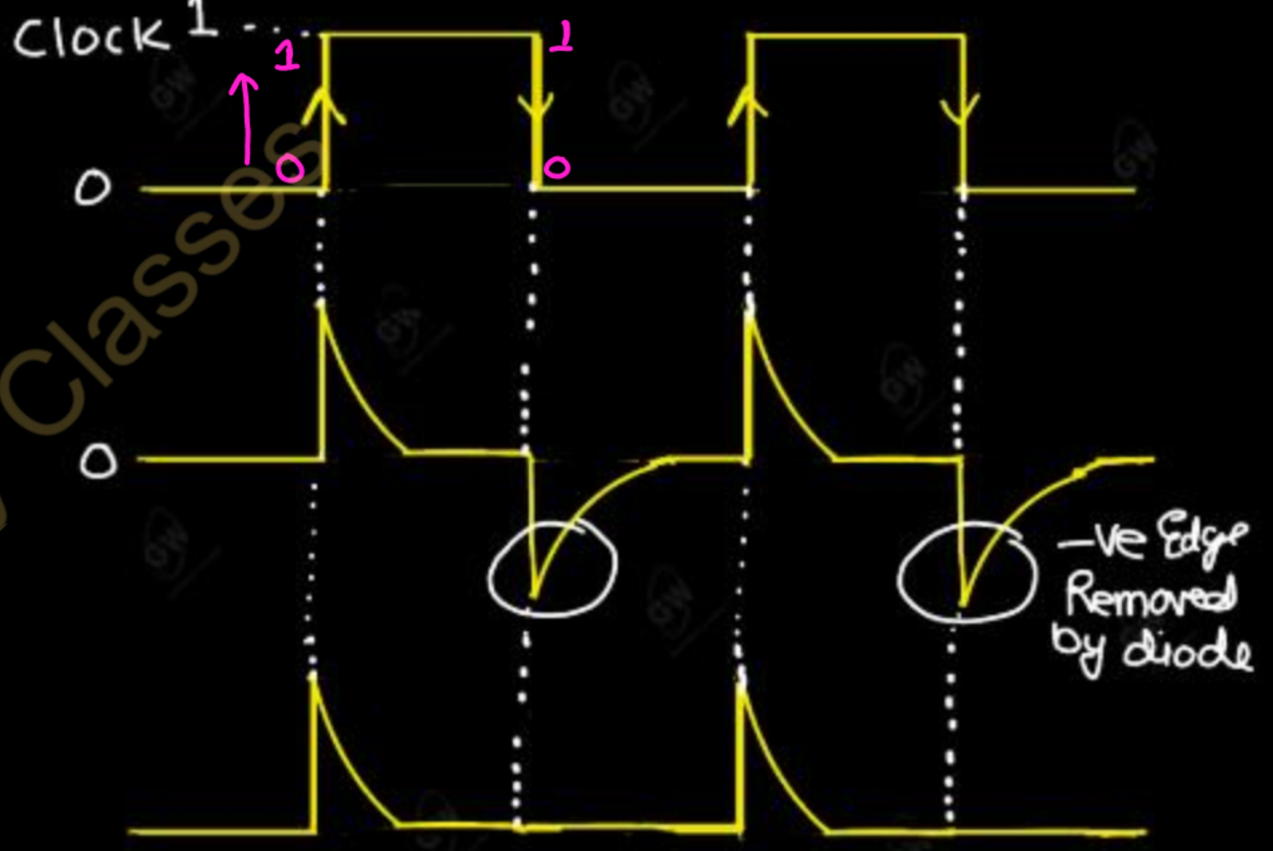
0 → 1 → +ve edge, rising.
1 → 0 → -ve edge, falling

- The input of flip flop is governed by flip flop in two ways .
  - (i) Positive Edge Triggered Flip Flop
  - (i) Negative Edge Triggered Flip Flop



↳ Differentiator

Clock Edge triggered Circuit



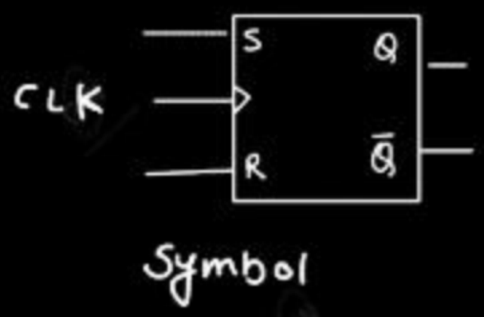
Positive Edge triggered pulse.

Gateway Classes

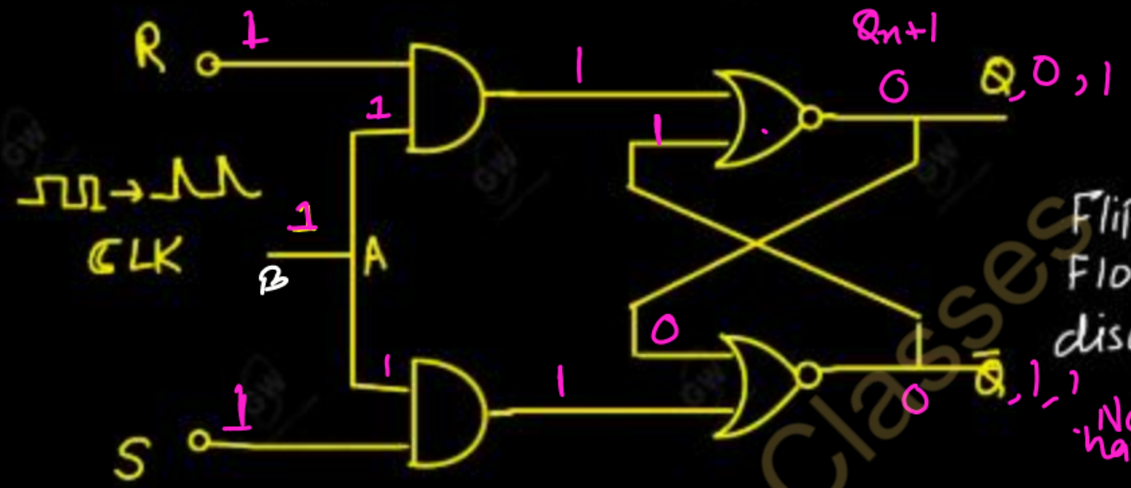
Positive edge Triggered SR Flip Flops

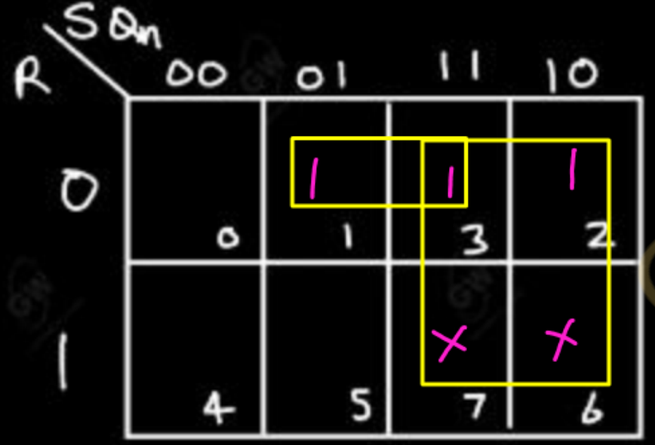
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SR flip-flop operates with only positive clock transitions.



Symbol





$Q_{n+1} = S + \bar{R}Q_n$

Characteristic Equation

CLK	R	S	Q_n Present State Q_n	Q_{n+1} Next State (Q_{n+1})
0	x	x	Q_n	Q_n
⌋	x	x	Q_n	Q_n
↓	x	x	Q_n	Q_n
↑	0	0	0 ✓	0
↑	0	0	1 ✓	1
↑	0	1	0	1
↑	0	1	1	1
↑	1	0	0	0
↑	1	0	1	0
↑	1	1	0	X
↑	1	1	1	X

Flip Flop disabled

No change

Set

Flip flop Enabled for +ve Edge

Reset

invalid

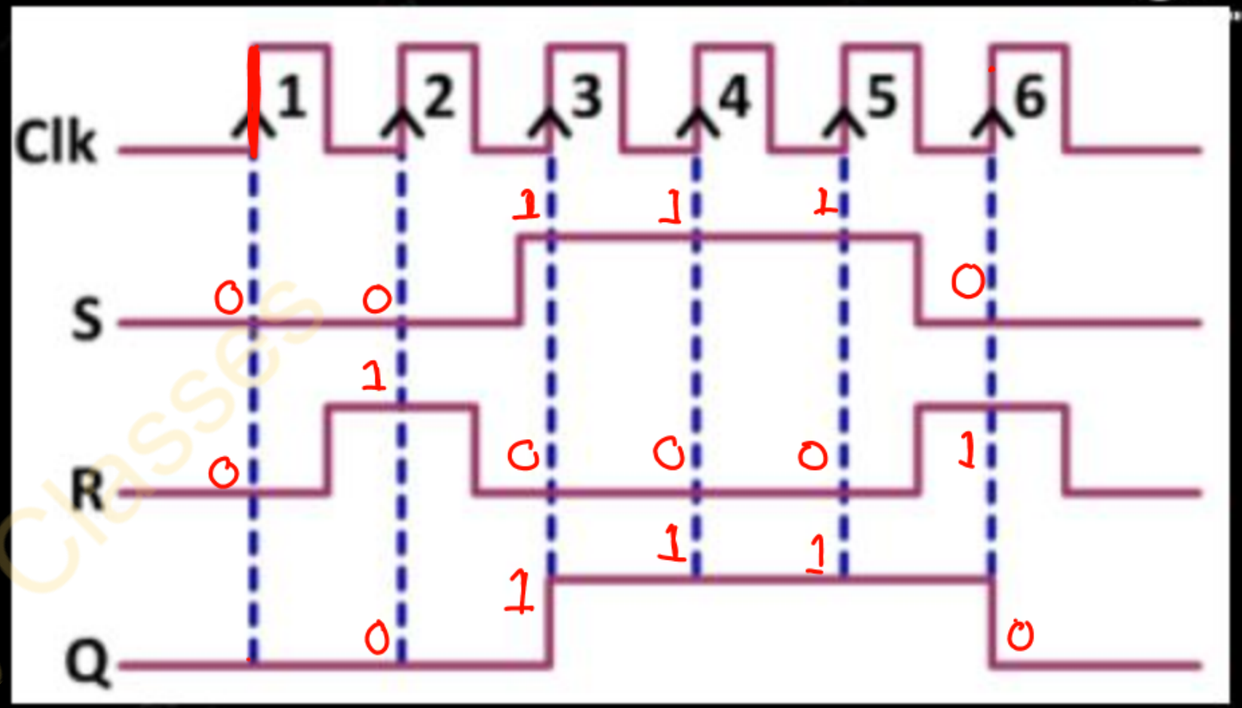
Gateway Classes

Wave Form

The output waveform is shown and is explained as follows

1. During the 1st positive clock edge, S=R=0 so Q =0
2. During 2nd positive clock edge, S=0 and R=1, Q =0 .
3. During 3rd positive clock edge, S=1 and R=0, Q=1.
4. During 4th positive clock edge, S=1 and R=0, Q=1

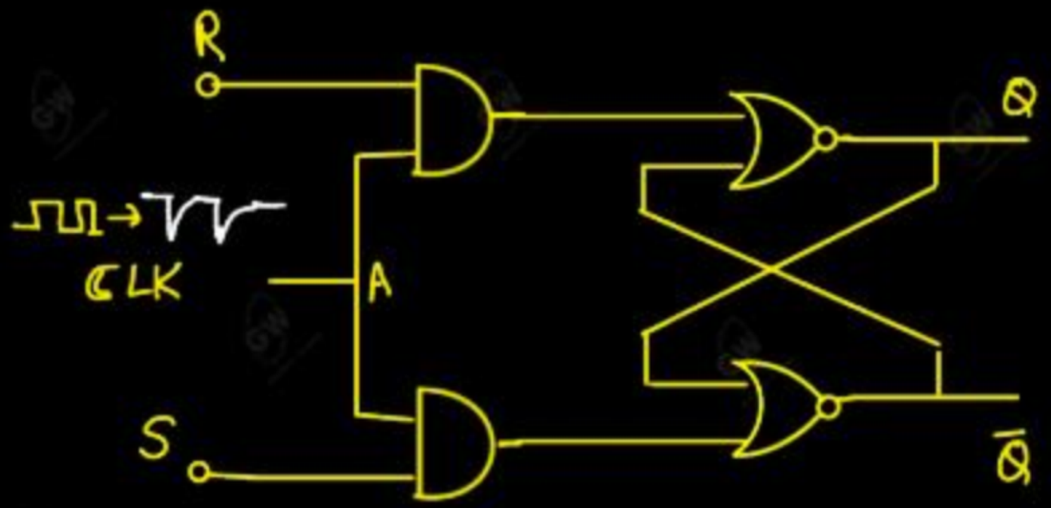
   Output is same at 5th clock pulse also .
5. During 6th positive clock edge, S=0 and R=1, Q=0

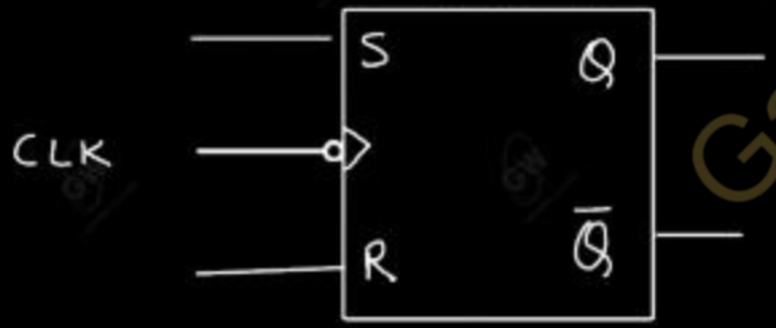


Gateway Classes

Negative edge Triggered SR Flip Flops

SR flip-flop operates with only negative clock transitions.





CLK	R'	S'	Present State Q_n	Next State (Q_{n+1})
0	x	x	Q_n	Q_n
1	x	x	Q_n	Q_n
↑	x	x	Q_n	Q_n
↓	0	0	0	0
↓	0	0	1	1
↓	0	1	0	1
↓	0	1	1	1
↓	1	0	0	0
↓	1	0	1	0
↓	1	1	0	x
↓	1	1	1	x

Flip Flop disabled

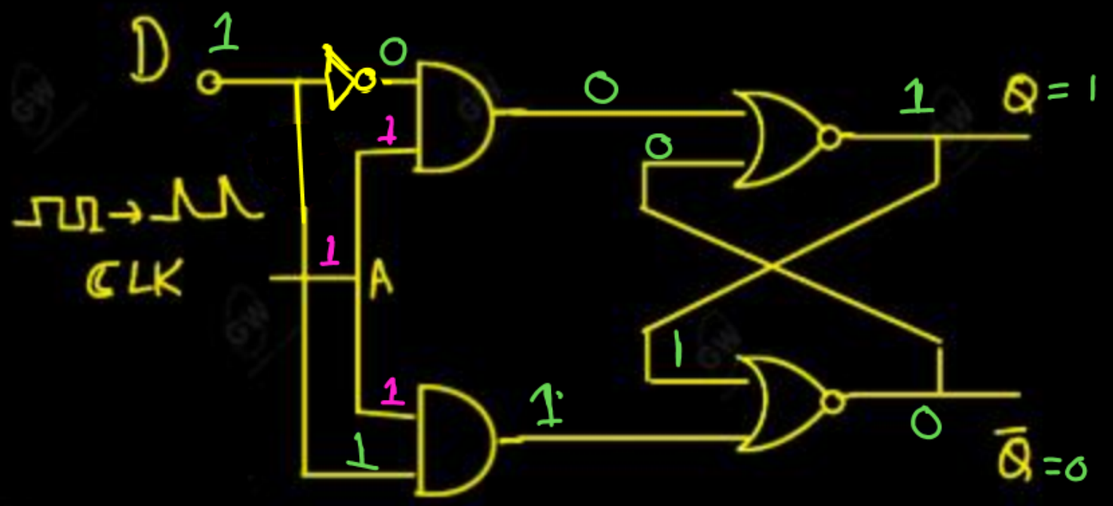
Flip flop Enabled for +ve Edge

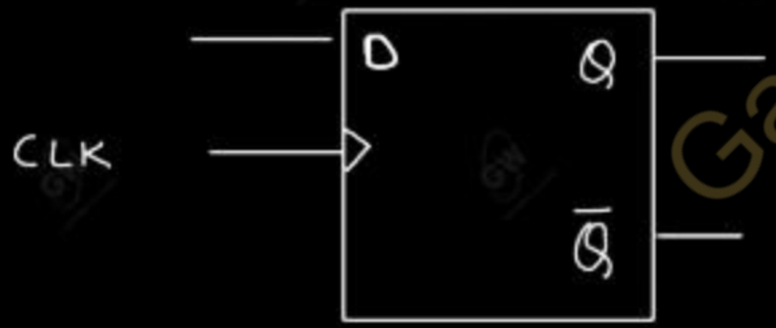
Gateway Classes

Positive edge Triggered D Flip Flops

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flip-flop operates with only positive clock transitions.

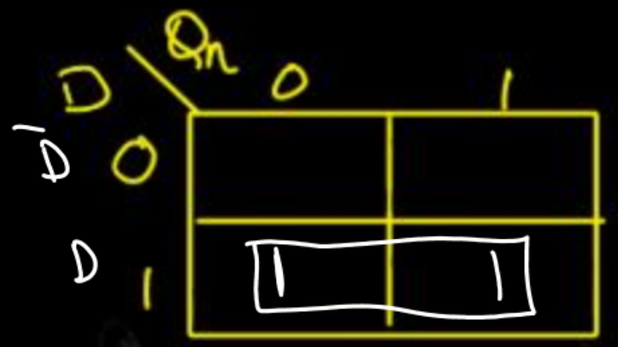




CLK	D	Present state Q_n	Next State (Q_{n+1})
0	x	Q_n	Q_n
⌋	x	Q_n	Q_n
↓	x	Q_n	Q_n
↑	0	0	0
↑	0	1	0
↑	1	0	1
↑	1	1	1

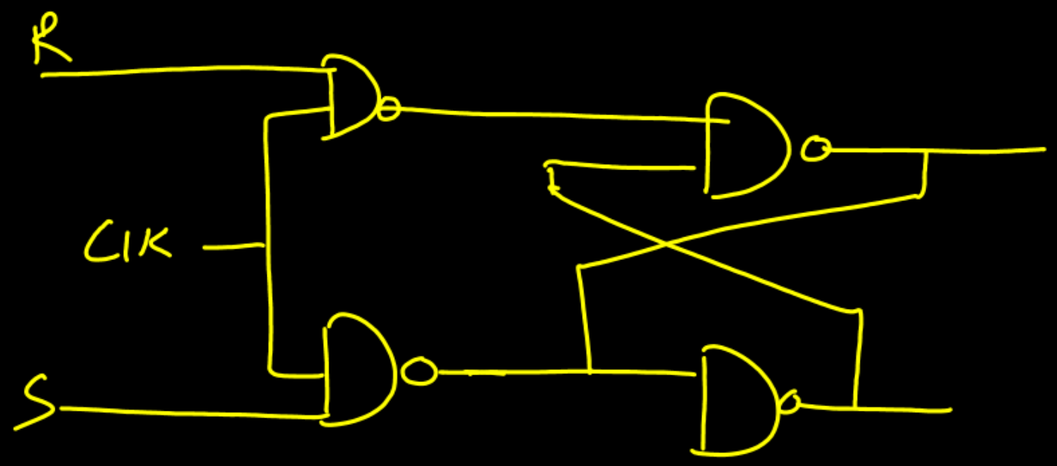
Flip Flop disabled

Flip flop Enabled for +ve Edge



$Q_{n+1} = D$

Gateway Classes



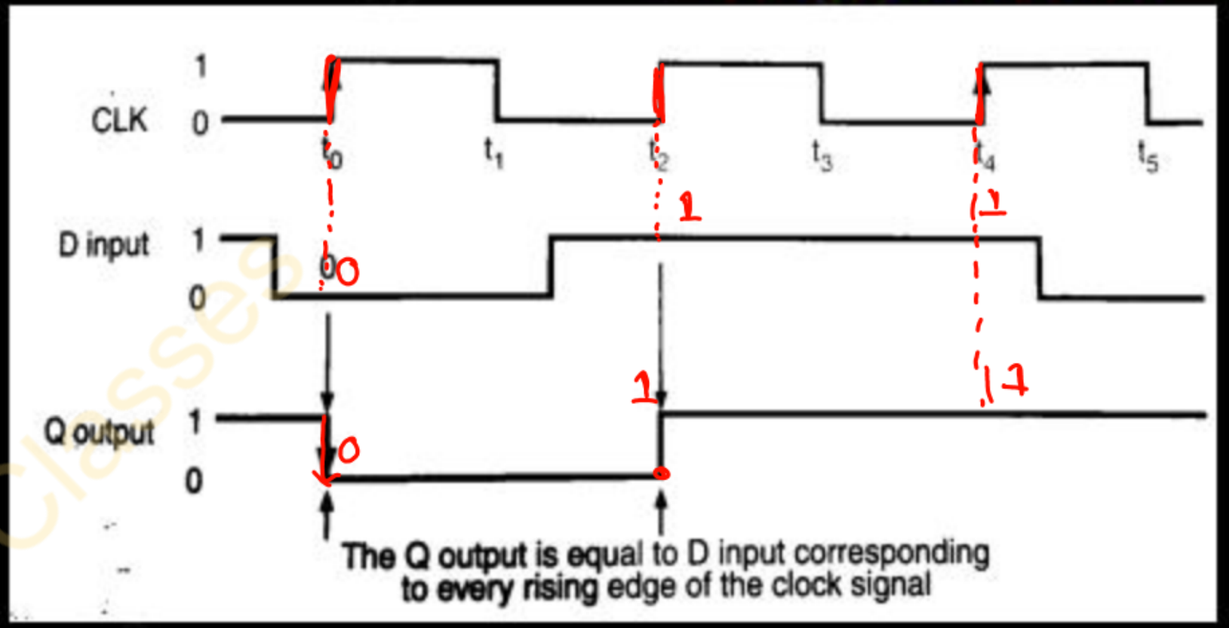
Gateway Classes

Positive edge Triggered D Flip Flop Waveform

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The output waveform is shown and is explained as follows

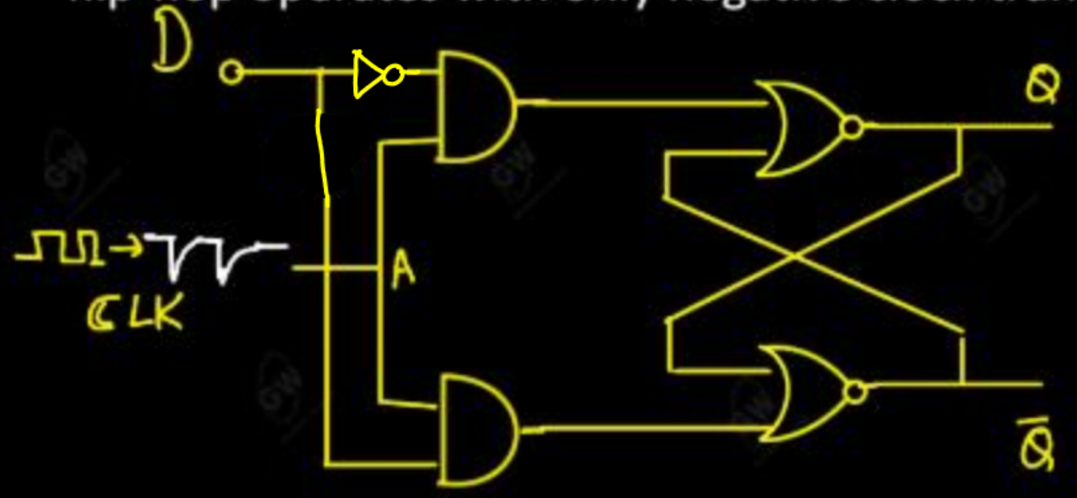
1. 1st Positive clock edge, D=0 so the output which is initially high will now change to logic 0.
2. 2nd Positive clock edge, D=1 so the output goes high.
3. 3rd Positive clock edge, D=1 so the output is still high.
4. 4th Positive clock edge, D=1 so the output goes high.

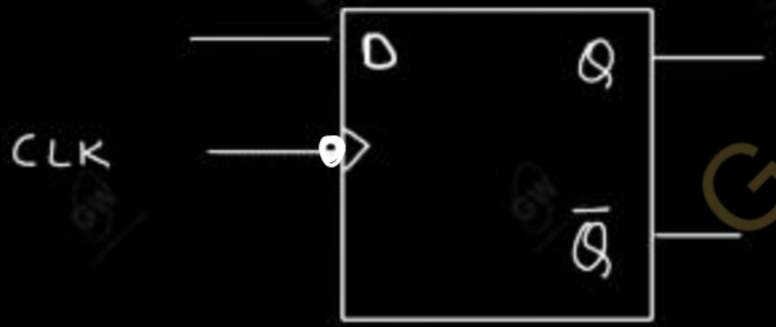


Gateway Classes

Negative edge Triggered D Flip Flops

flip-flop operates with only negative clock transitions.





CLK	D	Q_n Present State Q_n	Q_{n+1} Next State (Q_{n+1})
0	x	Q_n	Q_n
1	x	Q_n	Q_n
↑	x	Q_n	Q_n
↓	0	0	0
↓	0	1	0
↓	1	0	1
↓	1	1	1

Flip Flop disabled

Flip flop Enabled for −ve Edge

CLK	D	Q_n	Q_{n+1}
⊓	0	0	0
⊓	0	1	0
⊓	1	0	1
⊓	1	1	1

Gateway Classes

Negative edge Triggered D Flip Flop Waveform

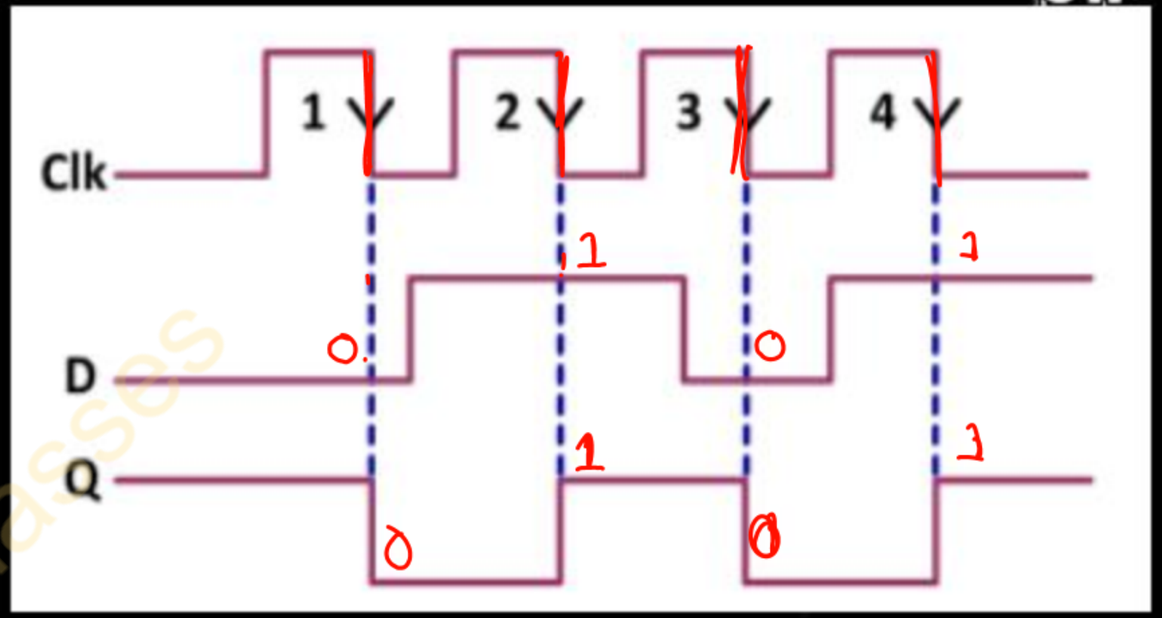
The output waveform is shown and is explained as follows

1. 1st negative clock edge, D=0 so the output which is initially SET will now change to logic 0.

2. 2nd negative clock edge, D=1 so the output goes high.

3. 3rd negative clock edge, D=0 so the output goes low.

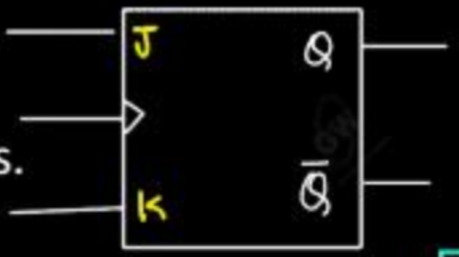
4. 4th negative clock edge, D=1 so the output goes high.



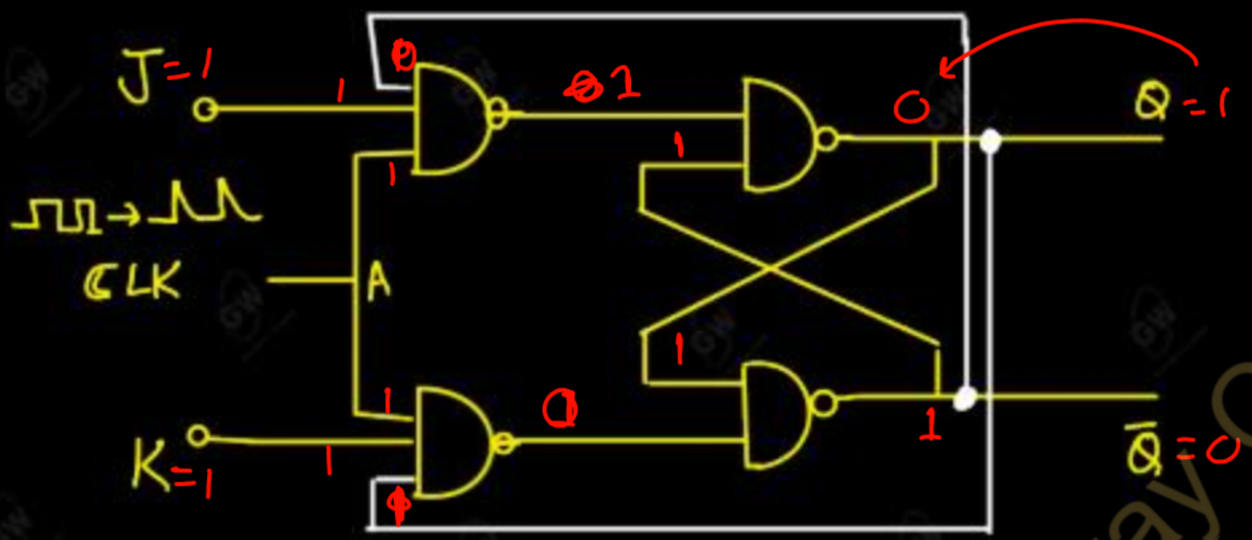
Gateway Classes

Positive edge Triggered JK Flip Flops

- JK flip-flop operates with only positive clock transitions.



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CLK	J	K	Q_n Present State Q_n	Q_{n+1} Next State (Q_{n+1})
0	x	x	Q_n	Q_n
⌋	x	x	Q_n	Q_n
↓	x	x	Q_n	Q_n
↑	0	0	0	0
↑	0	0	1	1
↑	0	1	0	0
↑	0	1	1	0
↑	1	0	0	1
↑	1	0	1	1
↑	1	1	0	1
↑	1	1	1	0

Flip Flop disabled

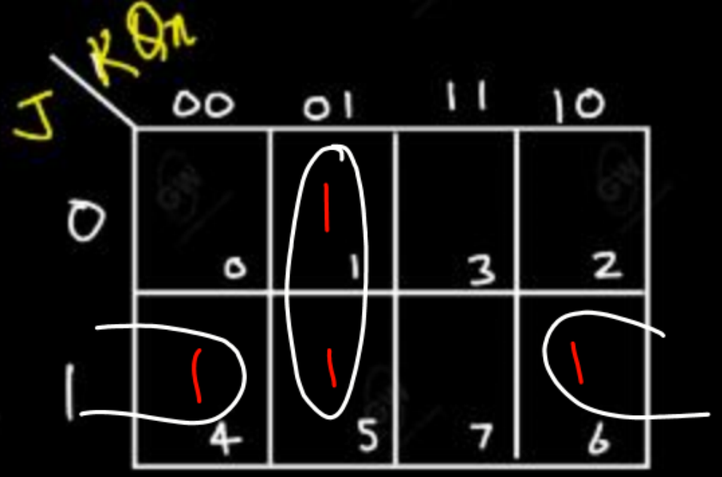
No change

Reset

Flip flop Enabled for +ve Edge

Set

Toggle

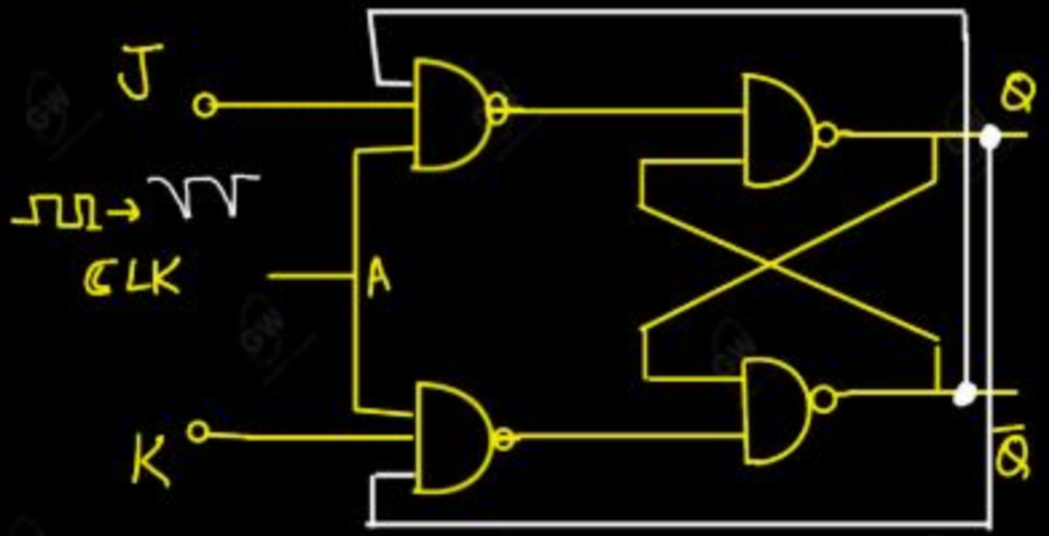


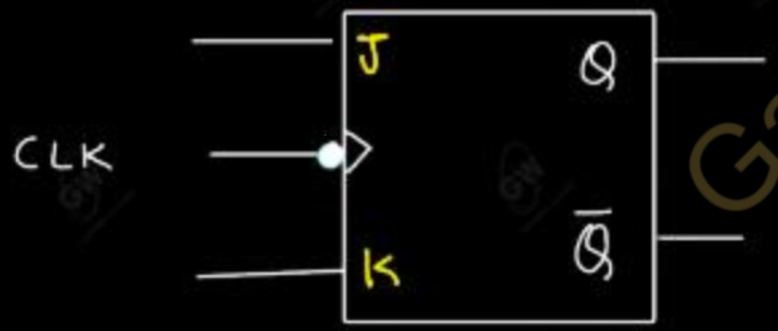
$$Q_{n+1} = \bar{K}Q_n + J\bar{Q}_n$$

Gateway Classes

Negative edge Triggered JK Flip Flops

JK flip-flop operates with only negative clock transitions.





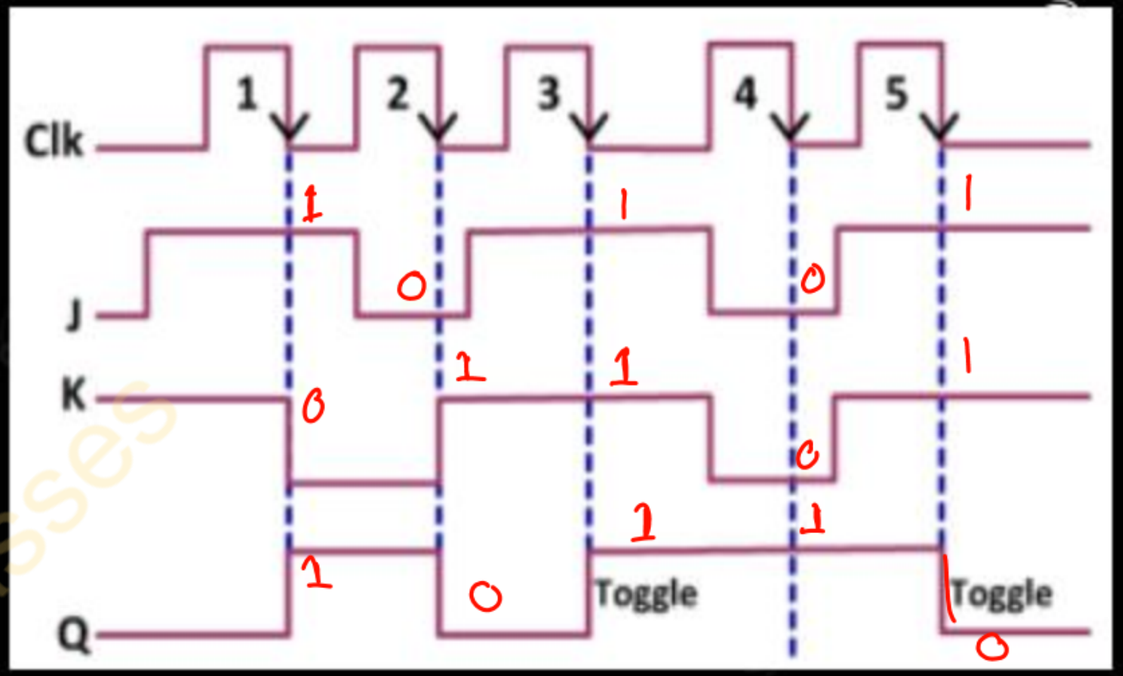
			Q_n	Q_{n+1}
CLK	J	K	Present State Q_n	Next State (Q_{n+1})
0	x	x	Q_n	Q_n
1	x	x	Q_n	Q_n
↑	x	x	Q_n	Q_n
↓	0	0	0	0
↓	0	0	1	1
↓	0	1	0	0
↓	0	1	1	0
↓	1	0	0	1
↓	1	0	1	1
↓	1	1	0	1
↓	1	1	1	0

Flip Flop disabled

Flip flop Enabled for +ve Edge

Gateway Classes

Negative edge Triggered JK Flip Flop waveform



The output waveform is shown and is explained as follows

1. 1st negative clock edge, J=1 and K=0 so the output which is initially RESET will now change to logic 1.

2. 2nd negative clock edge, J=0 and K=1 so the output goes low.

3. 3rd negative clock edge, J=K=1 so the output toggles i.e. initially it was in low state now the output goes high.

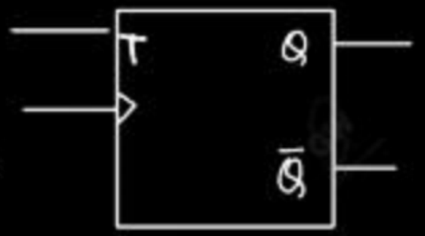
4. 4th negative clock edge, J=K=0 so the output retains its last value which is a high state.

5. 5th negative clock edge, J=K=1, the output will toggle, the last state was high so at 5th negative clock edge the output goes low.

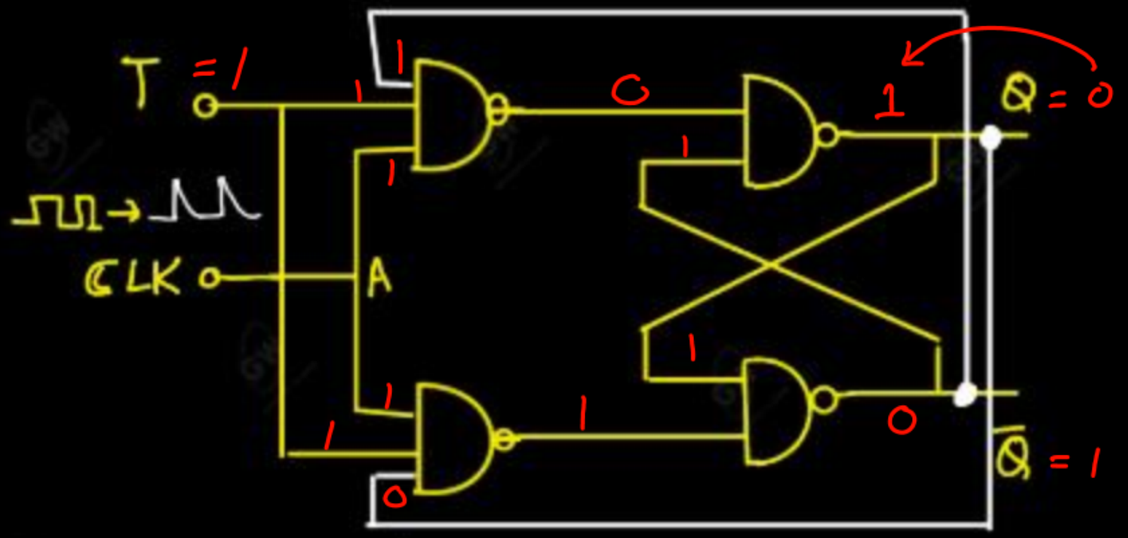
Gateway Classes

Positive edge Triggered T Flip Flops

- T flip-flop operates with only positive clock transitions.



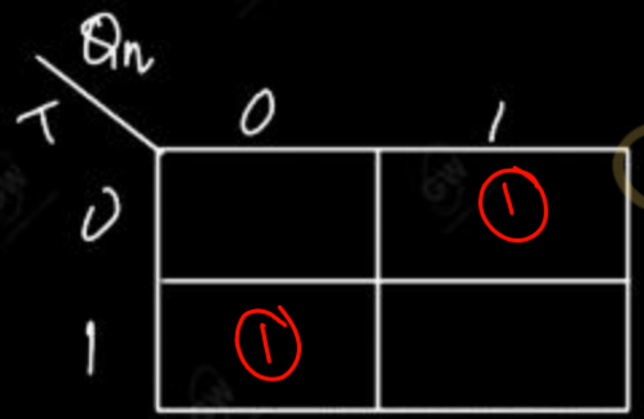
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CLK	T	Q_n Present State Q_n	Q_{n+1} Next State (Q_{n+1})
0	x	Q_n	Q_n
1	x	Q_n	Q_n
↓	x	Q_n	Q_n
↑	0	0	0
↑	0	1	1
↑	1	0	1
↑	1	1	0

Flip Flop disabled

No change ← Flip flop Enabled for +ve Edge

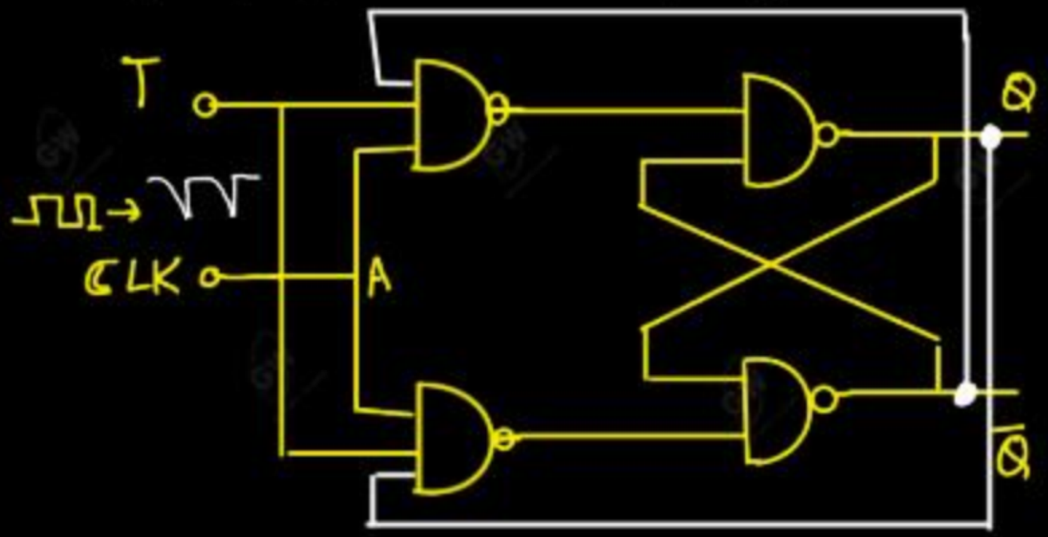


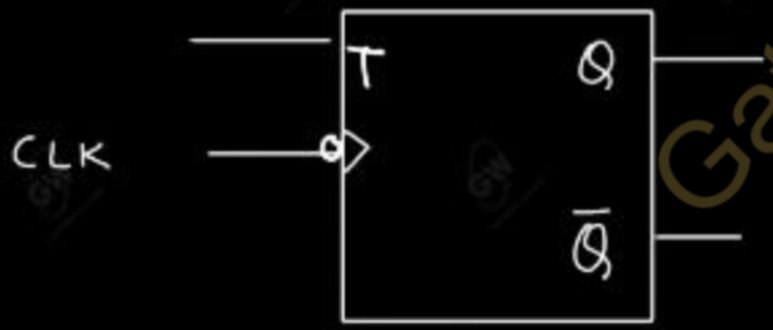
$$Q_{n+1} = \bar{T}Q_n + T\bar{Q}_n$$

Gateway Classes

Negative edge Triggered T Flip Flops

T flip-flop operates with only negative clock transitions.





CLK	T	Q_n Present state Q_n	Q_{n+1} Next State (Q_{n+1})	
0	x	Q_n	Q_n	Flip Flop disabled
1	x	Q_n	Q_n	
↑	x	Q_n	Q_n	
↓	0	0	0	Flip flop Enabled for −ve Edge
↓	0	1	1	
↓	1	0	1	
↓	1	1	0	

Gateway Classes

Excitation Table

An excitation table shows the required inputs of a flip-flop to make a desired transition from the present state (Q_n) to the next state (Q_{n+1}).

Excitation Table for SR Flip Flop

Truth Table

S	R	Q_n Present state Q_n	Q_{n+1} Next State (Q_{n+1})
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	0	x

Excitation Table →

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Gateway Classes

Excitation Table for D Flip Flop

Truth Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Gateway Classes

Excitation Table for JK Flip Flop

Truth Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Gateway Classes

Excitation Table for T Flip Flop

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

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