AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-3 Lec-3



Today's target

- Master Slave FF
- Flip Flop Conversion
- PYQ

Avinash Sir

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

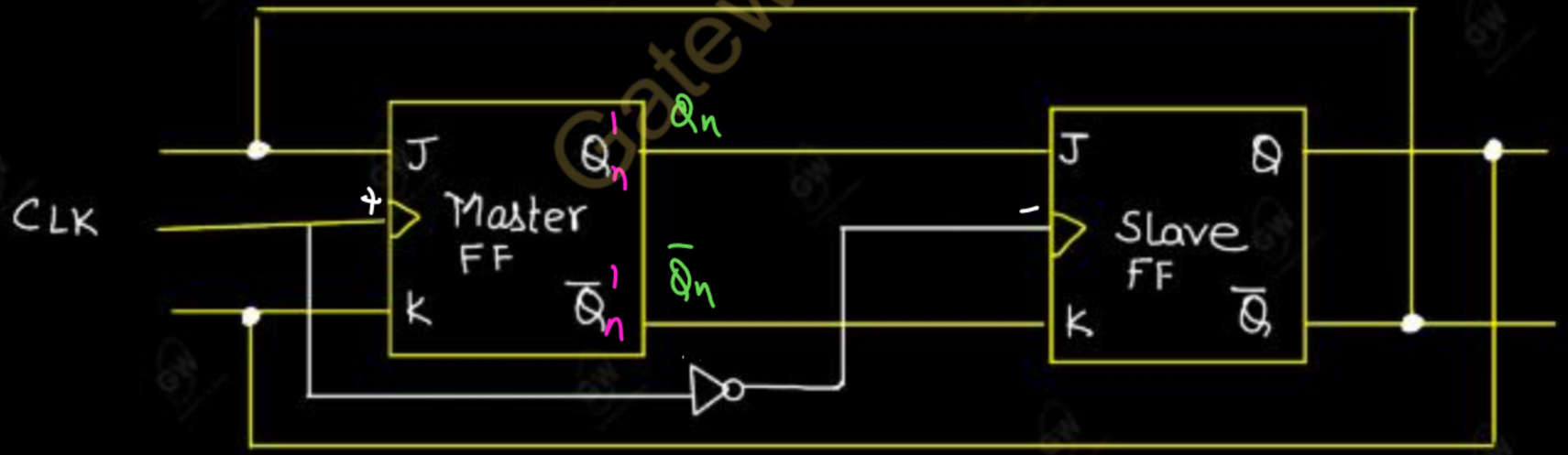
Master Slave Flip Flop

AKTU 2021-22

- Master-slave JK flip-flop is designed to eliminate the race around condition in JK flip-flop
- The first flip-flop is called the master, and it is driven by the positive clock cycle.
- The second flip-flop is called the slave, and it is driven by the negative clock cycle.
- During the positive clock cycle, master flip-flop gives the intermediate output but slave flip-flop will not give the final output.



- During the negative clock cycle, slave flip-flop gets activated and copies the previous output of the master flip-flop and produces the final output.



Gateway Classes

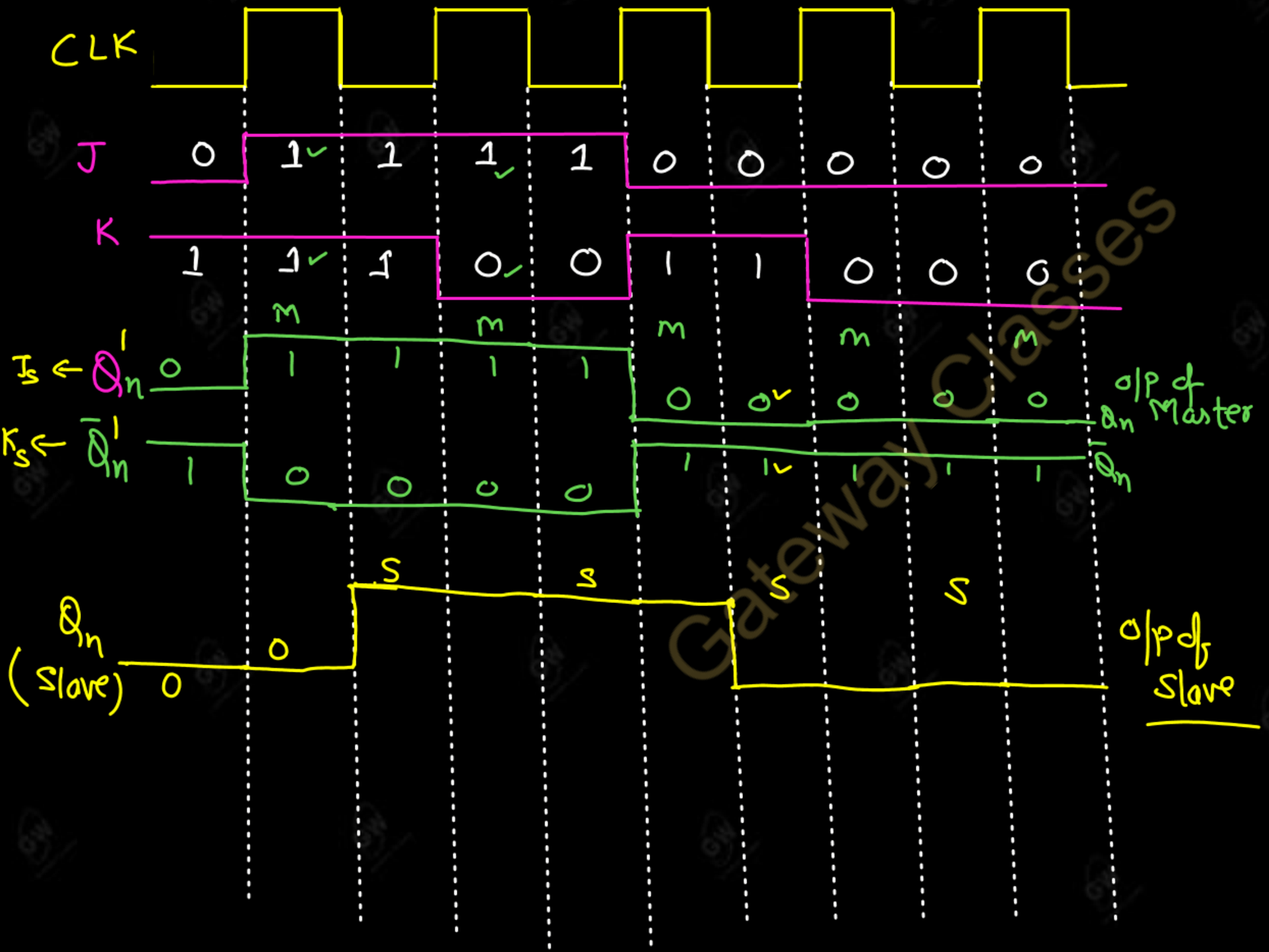
Master Slave JK Flip Flop Operation

Master flip flop responds before the slave flip flop.

- When J = 0 and K = 0, both JK flip flops remains inactive and hence the output Q remains unchanged. This is called Hold State of the master-slave JK flip flop.
- When J = 0 and K = 1, the output Q' of the master flip flop is high and goes to the input K of the slave flip flop. The clock signal forces the slave flip flop to reset. Therefore, the slave flip flop has the same output has the master flip flop, i.e., high Q' and low Q.
- When J = 1 and K = 0, the output Q of the master flip flop is high and goes to the input J of the slave flip flop, the negative transition of the clock signal sets the slave flip flop. Hence, this is called the set state of the master-slave JK flip flop.
- When J = 1 and K = 1, for this input combination, the master flip flop toggles on the positive transition of the clock pulse and the slave flip flop toggles on the negative transition of the clock pulse. Hence, the problem of the race around condition of the JK flip flop is solved.

Gateway Classes

Master Slave JK Flip Flop



Truth Table

CLK	J	K	Q_{n+1}	$\bar{Q}_{n+1}$
x	x	x	Q_n	$\bar{Q}_n$
1	0	0	Q_n	$\bar{Q}_n$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\bar{Q}_n$	Q_n

Flip Flop Conversion

Each flip-flop type has its own characteristic table (how inputs affect output).To convert one type to another:

- Write the characteristic table of the desired flip-flop.
- Write the excitation table of the given flip-flop.
- Compare both to find the required input combinations.
- Simplify using K-maps to get excitation equations.

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Flip Flop Conversion From SR to D

Required — Converted from

D	Q_n	Q_{n+1}	S	R
0	0	0	0	x
1	0	1	1 ✓	0
0	1	0	0	1
1	1	1	x ✓	0

Truth Table — Excitation Table

S ↓

D \ Q_n	0	1
0		
1	1	X

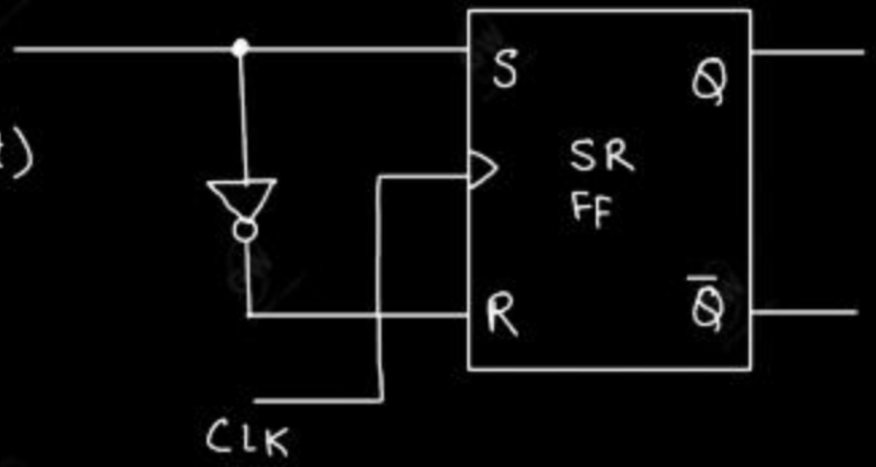
$S = D$

R ↓

D \ Q_n	0	1
0	X	1
1		

$R = \bar{D}$

Logic Diagram



"SR Flip flop to D FF"

GatewayClasses

Flip Flop Conversion From JK to T

Requir → Convert

T	Q_n	Q_{n+1}	J	K
0	0	0	0	x
1	0	1	1	x
1	1	0	x	1
0	1	1	x	0

Truth Table for T

Excitation Table for JK

J

T \ Q_n	0	1
0		x
1	1	x

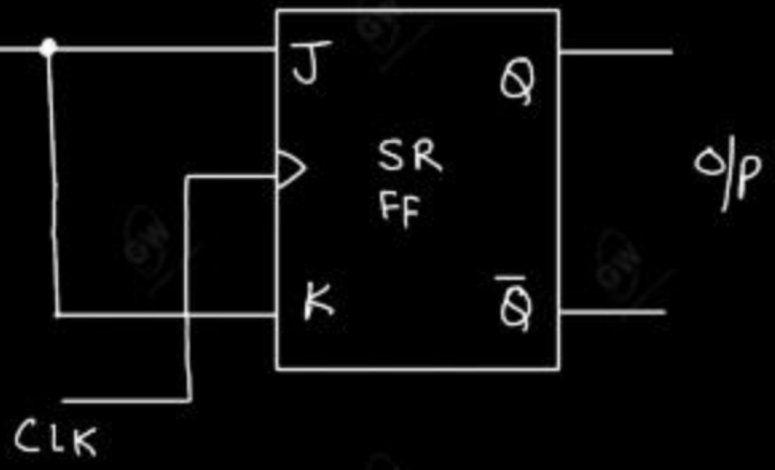
J = T

K

T \ Q_n	0	1
0	x	
1	x	1

K = T

Logic Diagram



"JK Flip flop to T FF"

Gateway Classes

Flip Flop Conversion From T to D

D	Q_n	Q_{n+1}	T
0	0	0	0
1	0	1	1
0	1	0	1
1	1	1	0

T.T

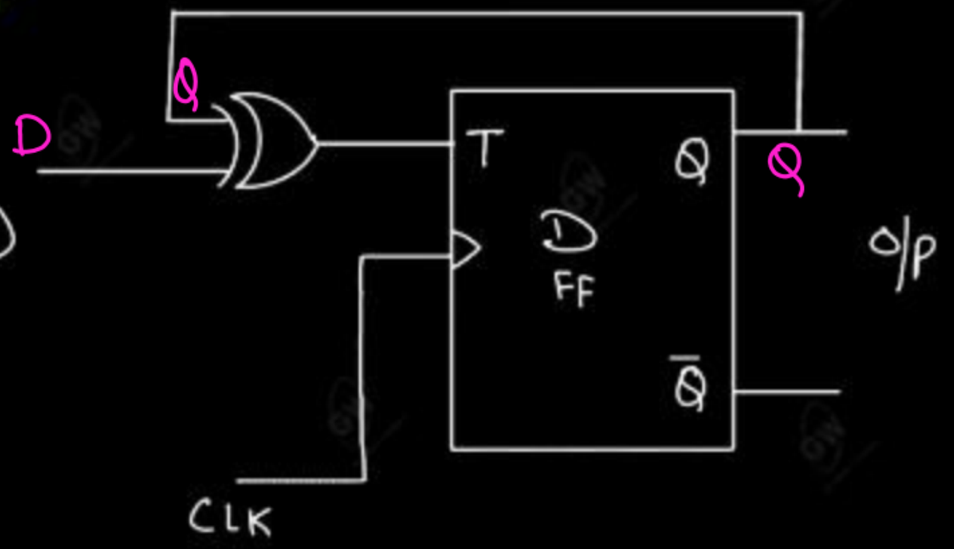
E.T.

T

D \ Q_n	0	1
0		1
1	1	

$T = \bar{D}Q_n + D\bar{Q}_n = D \oplus Q_n$

Logic Diagram



"D Flip flop to T FF"

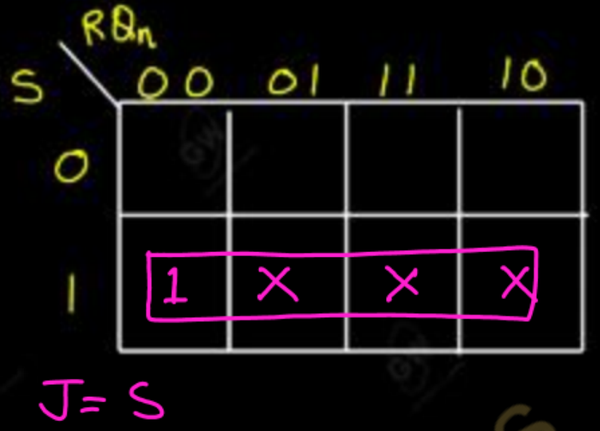
Gateway Classes

Flip Flop Conversion From JK to SR

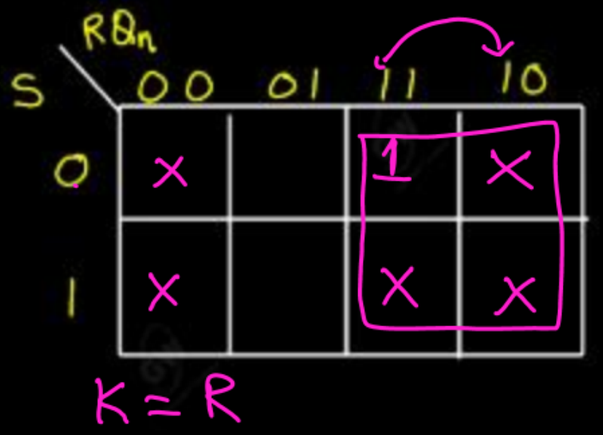
S	R	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
0	1	0	0	0	x
1	0	0	1	1	X
1	1	0	1	x	X
0	0	1	0	X	0
0	1	1	0	X	1
1	0	1	1	x	0
1	1	1	1	X	x

T·T SR

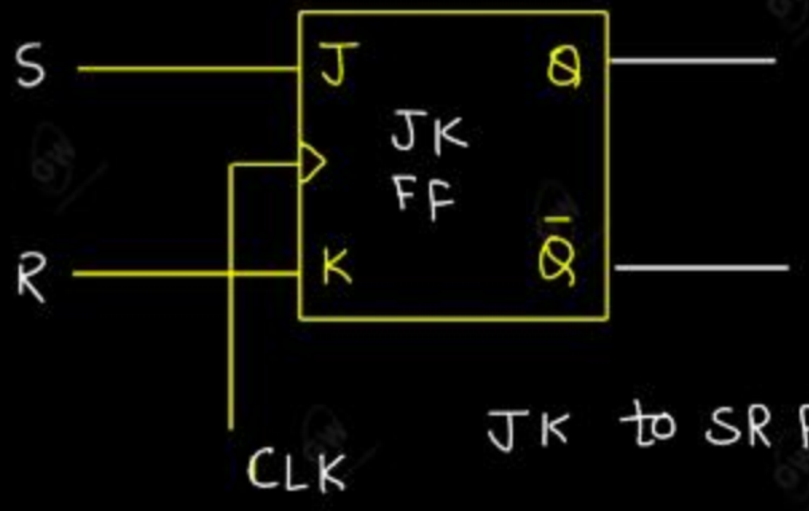
E·T JK



J = S



K = R



JK to SR FF

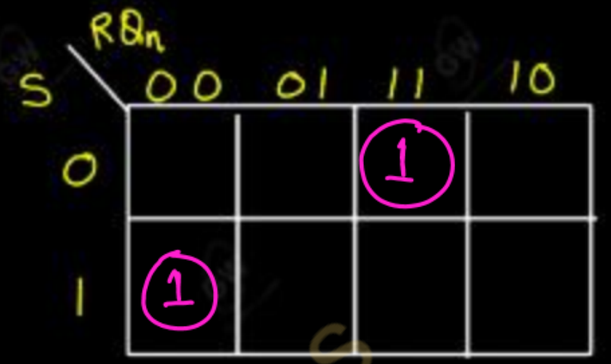
Gateway Classes

Flip Flop Conversion From T to SR

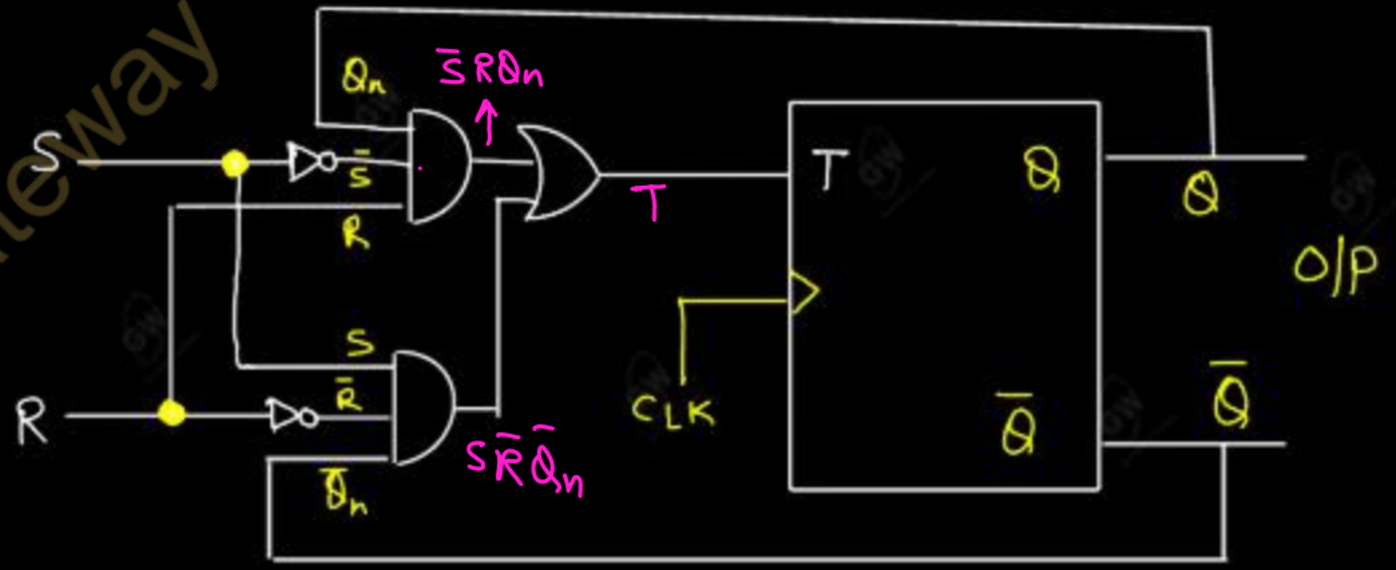
S	R	Q_n	Q_{n+1}	T
0	X	0	0	0
1	0	0	1	1 ✓
0	1	1	0	1 ✓
X	0	1	1	0

T·T(SR)

(Ē·T) T



$T = S\bar{R}\bar{Q}_n + \bar{S}RQ_n$



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Thank You

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