AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design



Unit-3 Lec-6

Today's target

- Mealy and Moore machines,
- State diagrams, state reduction,
- Analysis of clocked sequential circuits,
- Design of clocked sequential circuits.
- PYQ

Avinash Sir

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

State & State Variable:- State is defined by the output of Flip flop(Memory). And State Variables are the physical memory elements used in digital hardware to encode and store the current state of the FSM.

State and State Variables are related by the expression.

$$2^x = y$$

$2^2 = 4$



Where x= No. of Flip Flop (Memory) and Y is the Maximum number of possible state.



State Diagram :- A State Diagram is the graphical, visual representation of an FSM's behavior.

Nodes (Circles): Represent the states of the machine.

Arcs (Directed Edges/Arrows): Represent the transitions (movement) from one state to the next.

Labels: ***Mealy Machine:*** Labels on the arcs are in the format Input / Output (e.g., 1/0).

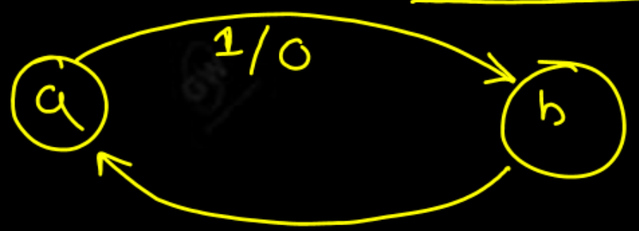
Moore Machine: Labels on the nodes are in the format State Name / Output (e.g., State A / 0), and the arcs are labeled only with the Input.

Starting State: Usually indicated by an arrow pointing into the node from nowhere.

Gateway Classes

Finite State Machine (FSM)

A synchronous sequential circuit is also called as Finite State Machine FSM, if it has a finite number of states.



Components of a Finite State Machine

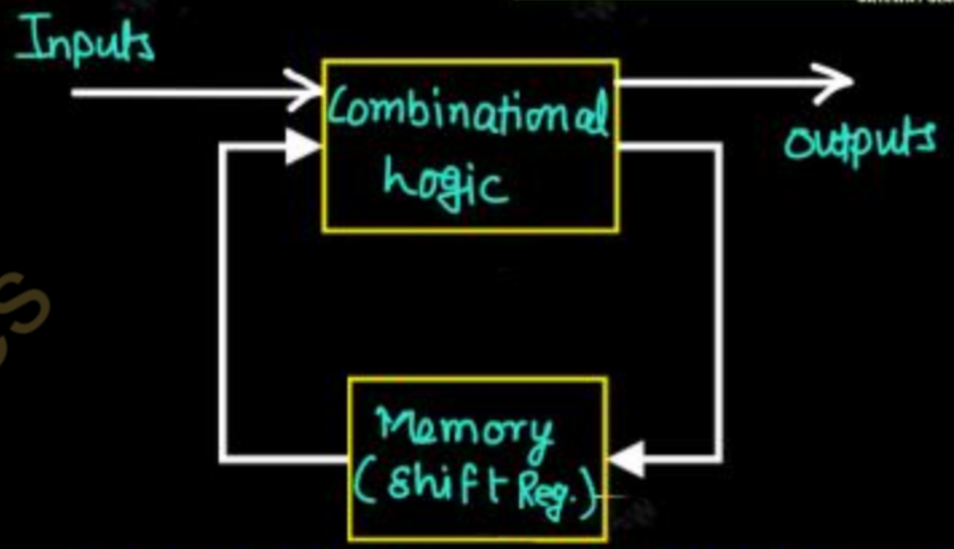
- **Finite States:-** The finite states are nothing but the distinct modes or conditions in the given system. Each finite states represents a specific behavior. They are represented by symbols or labels.
- **State Transitions:-** It is the change from one state to another. These are generally triggered by events which are associated with some rules or conditions and determine the next state of the system.
- **State Diagram:-** Behavior of a finite state machine can be represented in a graphical form known as state diagrams.
- **Inputs:** They trigger the state transitions in the system.
- **Outputs:-** The results produced by the system are known as outputs.

Gateway Classes

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FSMs are used in many digital system designs:

- Control units in microprocessors
- Traffic light controllers, Vending machines
- Sequence detectors
- Communication protocols (UART, I2C, etc.)
- Robotics and automation systems



Finite State Machine (FSM) Block Diagram

Advantages of FSM

- Easy to design and analyze.
- Reduces complexity in sequential circuit design.
- Provides a systematic way to represent control logic.
- Useful for both hardware and software implementations.

Limitations of FSM

- Becomes complex for large systems (many states).
- Requires careful state reduction and minimization. Memory usage increases with number of states.

Gateway Classes

Types of FSM

There are two main types of FSMs based on how the outputs depend on states and inputs:

Type	Output Depends On	Diagram Representation	Example
Moore Machine	Current State only	Output shown inside state circle	Sequence detector
Mealy Machine	Current State + Input	Output shown on transition line	Serial data detector

Gateway Classes

Moore Machine

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A Finite State Machine is said to be a Moore state machine, if its *outputs depend only on the present states*. There are two parts presents in a Moore state machine. Those are combinational logic and memory. In this case, the present inputs and present states determine the next states. So, based on next states, Moore machine produces the outputs. So, the outputs will be valid only after transition of the state.

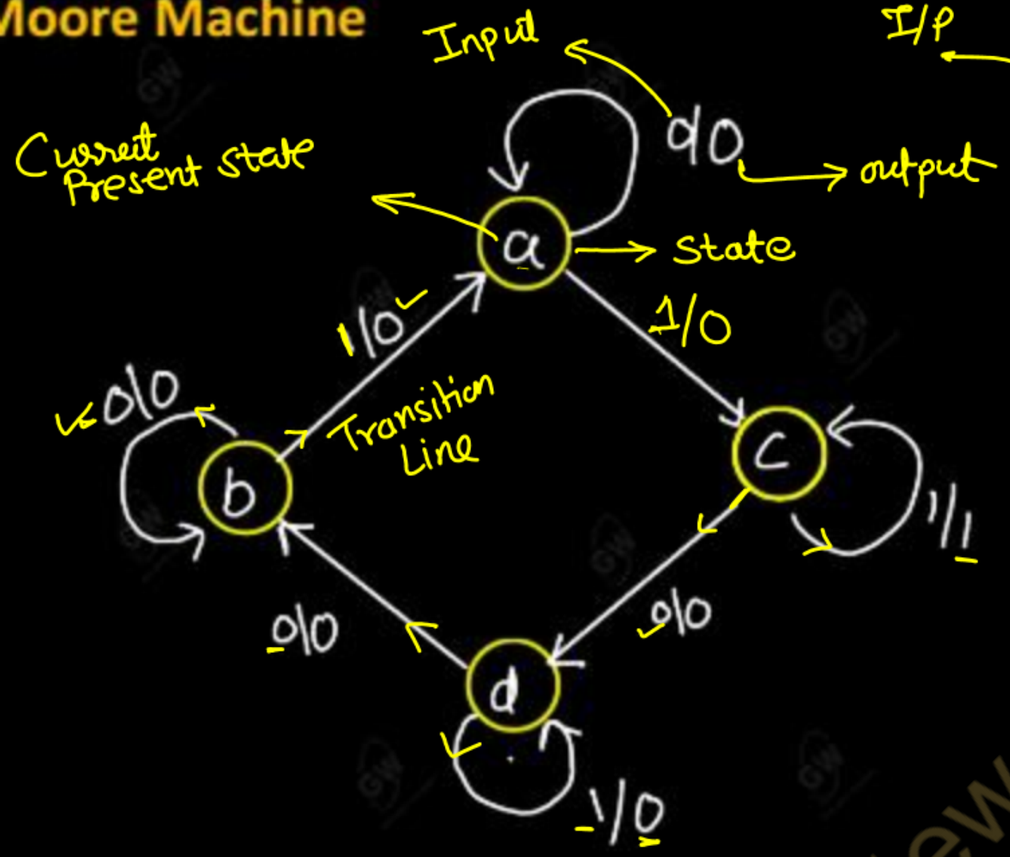
There are four states, namely A, B, C, and D. These states and the respective outputs are labelled inside the circles. Here, only the input value is labeled on each transition.



Gateway Classes

Moore Machine

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I/P 0 / 1 → o/p

Transition Table

Present state	Next state		output	
	x = 0	x = 1	x = 0	x = 1
a	a	c	0	0
b	b	a	0	0
c	d	c	0	1
d	b	d	0	0

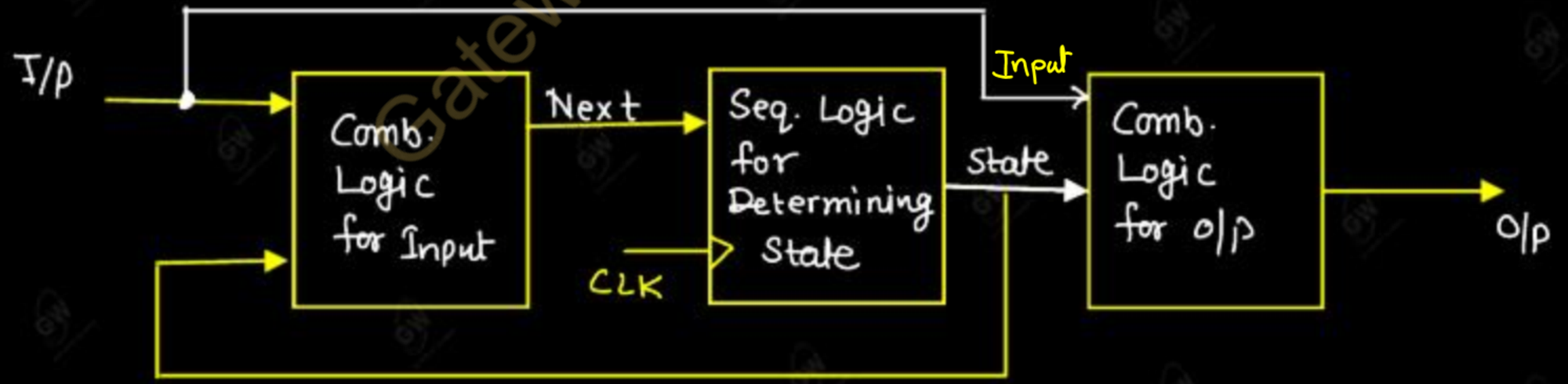
Gateway Classes

Mealy Machine

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In a Mealy state machine, outputs *depend on both present inputs & present states.* There are two main parts presents in the Mealy state machine. Those are combinational logic circuit and memory element. The memory element is useful to provide some part of previous outputs and present states as inputs to the combinational logic circuit.

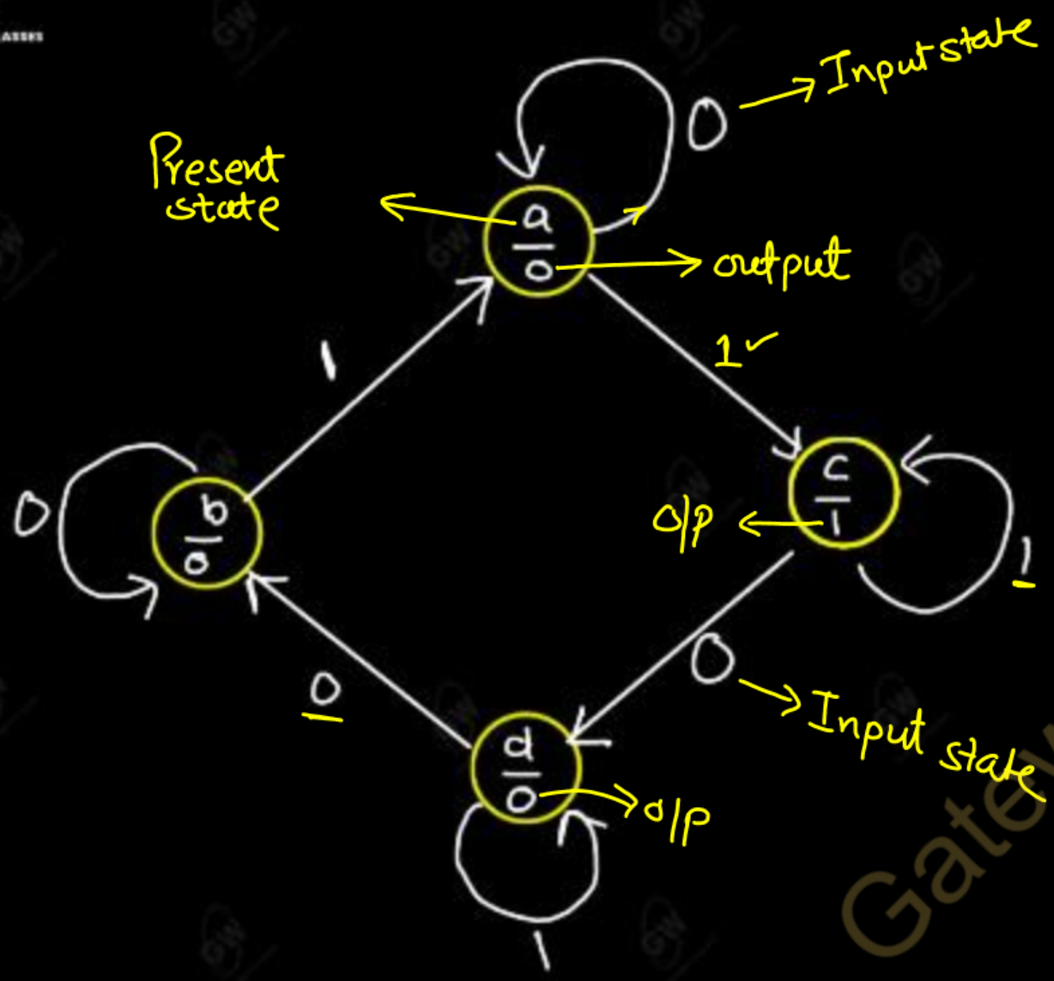
There are three states, namely A, B and C . Each state labelled inside the circles and each circle corresponds to one state. State transitions between these states are represented with directed lines. Here, 0 / 0, 1 / 0 and 1 / 1 denote the input / output. In the above figure, there are two state transitions from each state based on the value of input.



Gateway Classes

Mealy Machine

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Transition Table

Present state	Next state		Output
	x = 0	x = 1	
a	a	c	0
b	b	a	0
c	d	c	1
d	b	d	0

Gateway Classes

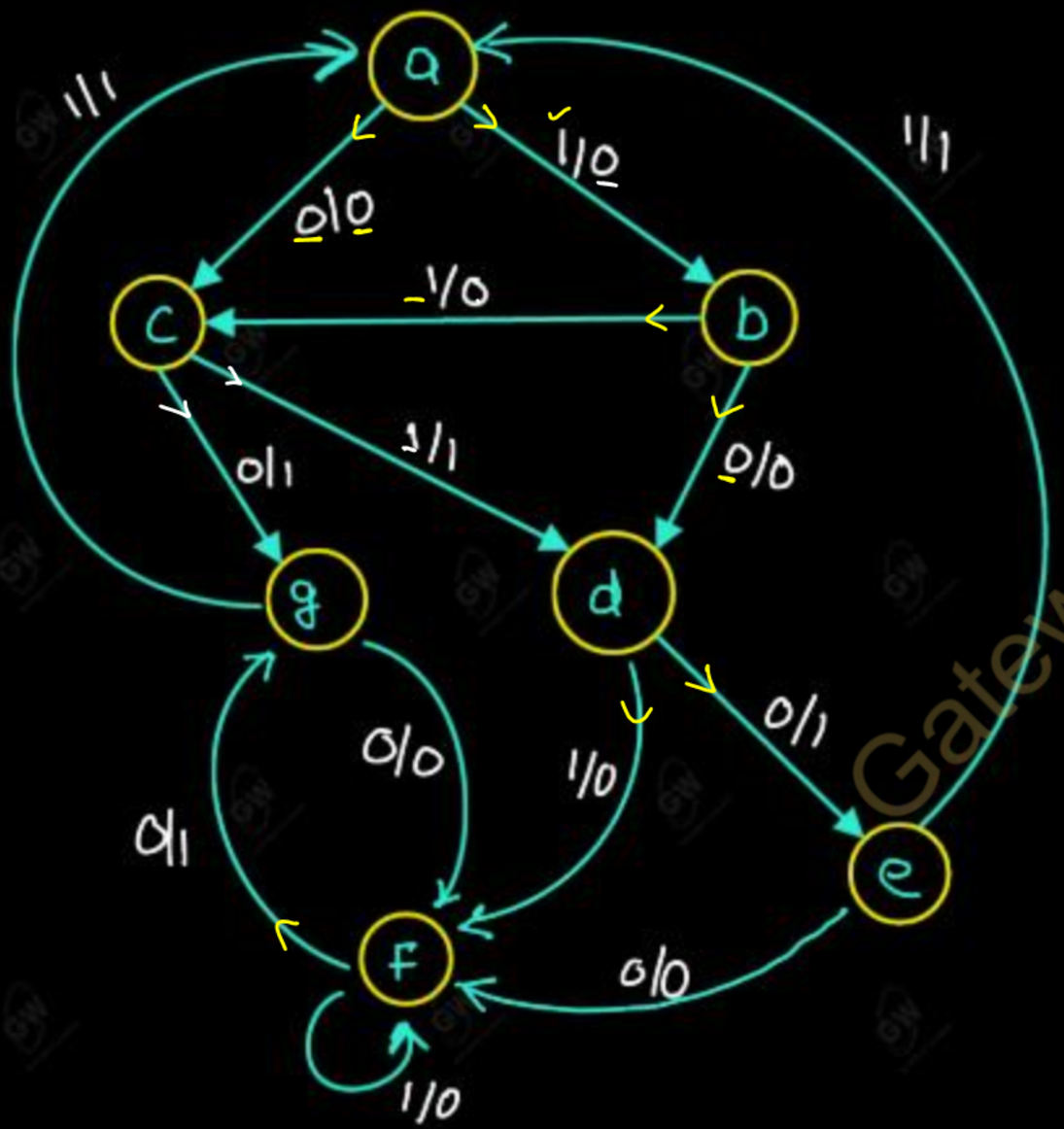
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Difference Between Mealy Machine and Moore Machine

Feature	Mealy Machine	Moore Machine
Output Dependency	Current state and current input	Current state only
Output Timing	Can change during a state transition, based on the input	Changes only when the state changes, synchronized with the clock
Reaction Speed	Faster response to input changes	Slower response, with a one-clock-cycle delay
Number of States	Usually requires fewer states for the same function	Usually requires more states
Design Complexity	Can be more complex to design	Is generally simpler to design
Hardware Requirement	Requires less hardware	Requires more hardware
Output Association	Outputs are associated with the transitions between states	Outputs are associated with the states themselves

Gateway Classes

State Diagram and State Reduction



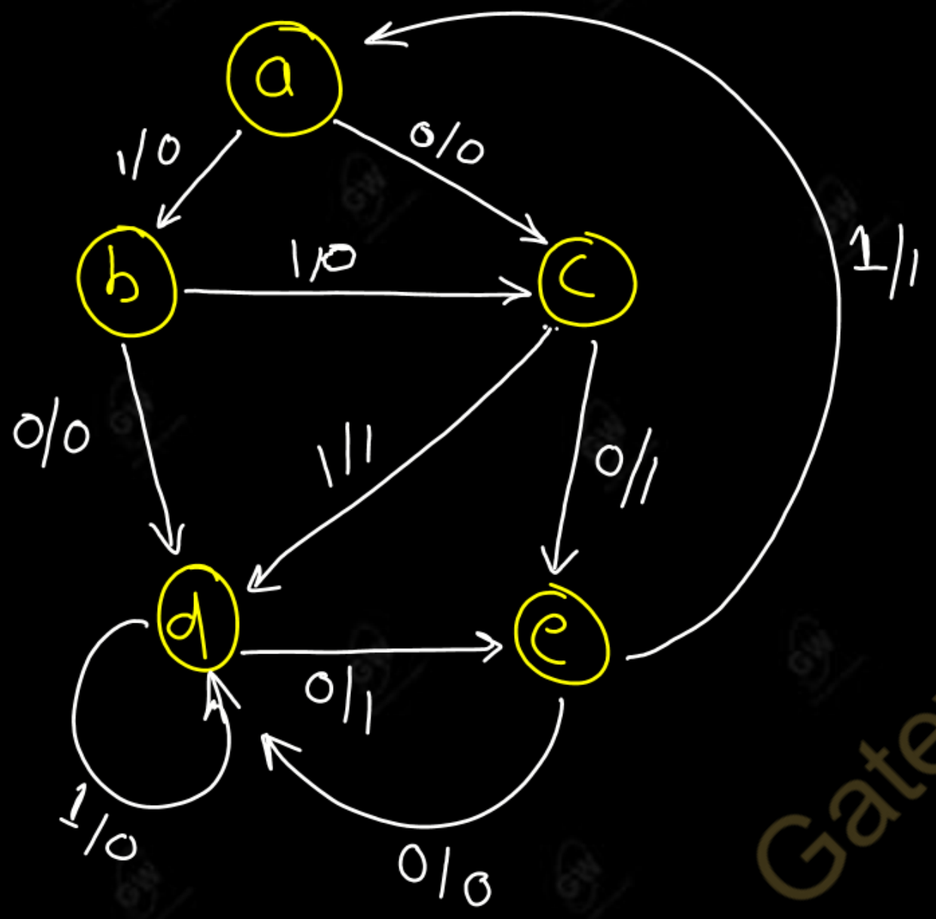
Transition Table

Present State	Next State		output	
	x = 0	x = 1	x = 0	x = 1
a	c	b	0	0
b	d	c	0	0
c	g(e)	d	1	1
d	e(g)	f(d)	1	0
e	f(d)	a	0	1
→ f	g	f	1	0
→ g	f	a	0	1

e = g , f = d

Gateway Classes

State Diagram and State Reduction



Reduced transition Table.

Present State	Next State		output	
	$x=0$	$x=1$	$x=0$	$x=1$
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	d	1	0
e	d	a	0	1

Gateway Classes

State Assignment

Present State	Next State		output	
	$x=0$	$x=1$	$x=0$	$x=1$
000	010	001	0	0
001	011	010	0	0
010	100	011	1	1
011	100	011	1	0
100	011	000	0	1

hot

a = 000 , b = 001 , c = 010

d = 011 , e = 100

No. of bit = 2

$2^2 = 4$

No. of bit = 3

$2^3 = 8$

Gateway Classes

Design Procedure of Circuit

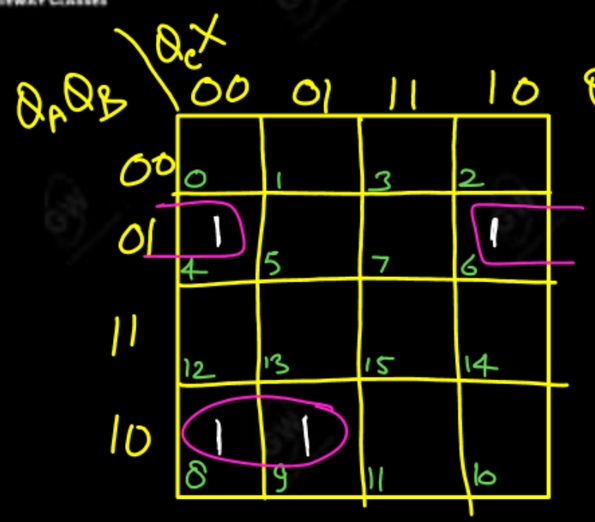
	Present state			Input	Next state			Inputs of flip flop		
	Q_A	Q_B	Q_C	X	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1	0
1	0	0	0	1	0	0	1	0	0	1
2	0	0	1	0	0	1	1	0	1	0
3	0	0	1	1	0	1	0	0	1	1
4	0	1	0	0	1	0	0	1	1	0
5	0	1	0	1	0	1	1	0	0	1
6	0	1	1	0	1	0	0	1	1	1
7	0	1	1	1	0	1	1	0	0	0
8	1	0	0	0	0	1	1	1	1	1
9	1	0	0	1	0	0	0	1	0	0

Excitation Table

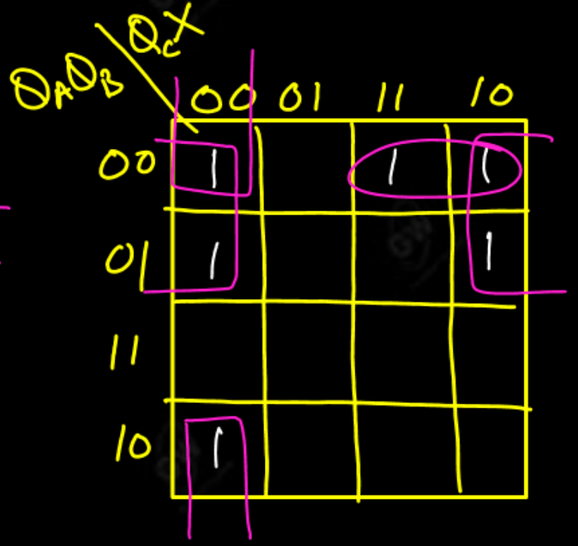
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Gateway Classes

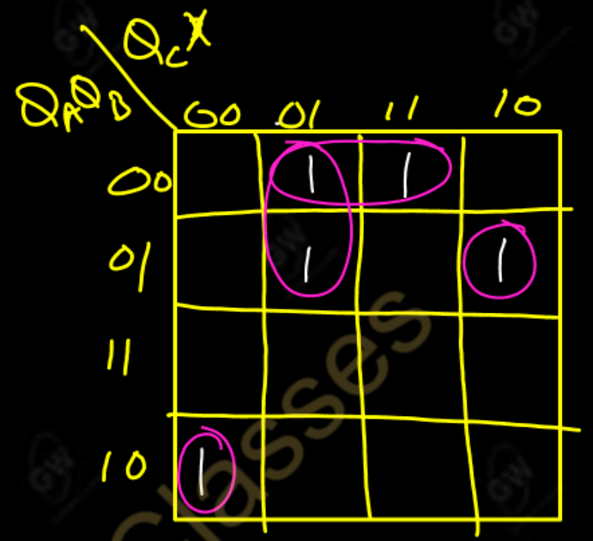
Design Procedure of Circuit



$$T_A = Q_A\bar{Q}_B\bar{Q}_C + \bar{Q}_AQ_B\bar{X}$$



$$T_B = \bar{Q}_A\bar{X} + \bar{Q}_AQ_C + \bar{Q}_B\bar{Q}_C\bar{X}$$



$$T_C = \bar{Q}_A\bar{Q}_BX + \bar{Q}_A\bar{Q}_CX + \bar{Q}_AQ_BQ_C\bar{X} + Q_A\bar{Q}_B\bar{Q}_C\bar{X}$$

Gateway Classes

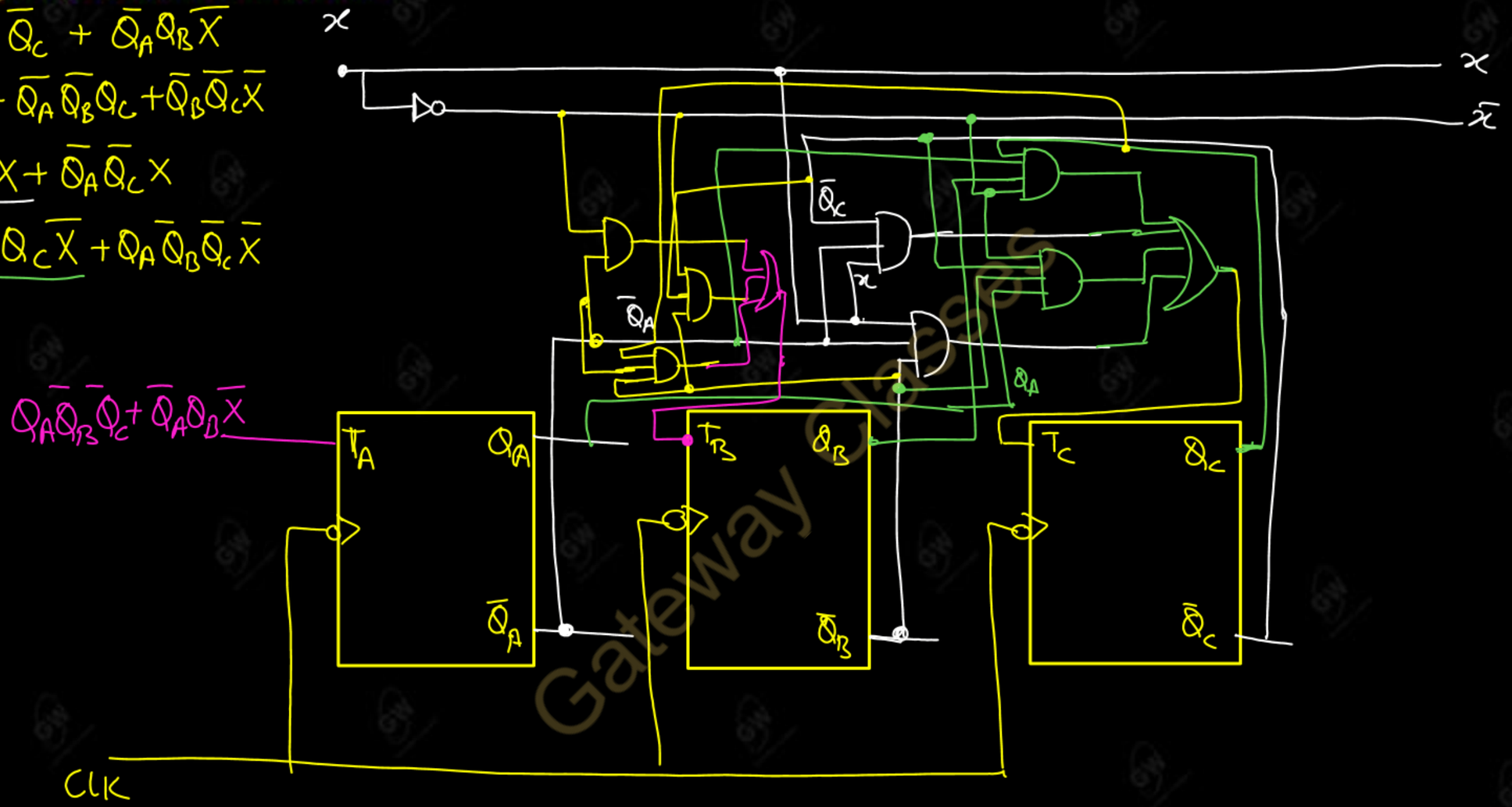
Design Procedure of Circuit

$$T_A = Q_A \bar{Q}_B \bar{Q}_C + \bar{Q}_A Q_B \bar{X}$$

$$T_B = \bar{Q}_A X + \bar{Q}_A \bar{Q}_B Q_C + \bar{Q}_B \bar{Q}_C X$$

$$T_C = \bar{Q}_A \bar{Q}_B X + \bar{Q}_A \bar{Q}_C X + \bar{Q}_A Q_B Q_C \bar{X} + Q_A \bar{Q}_B \bar{Q}_C X$$

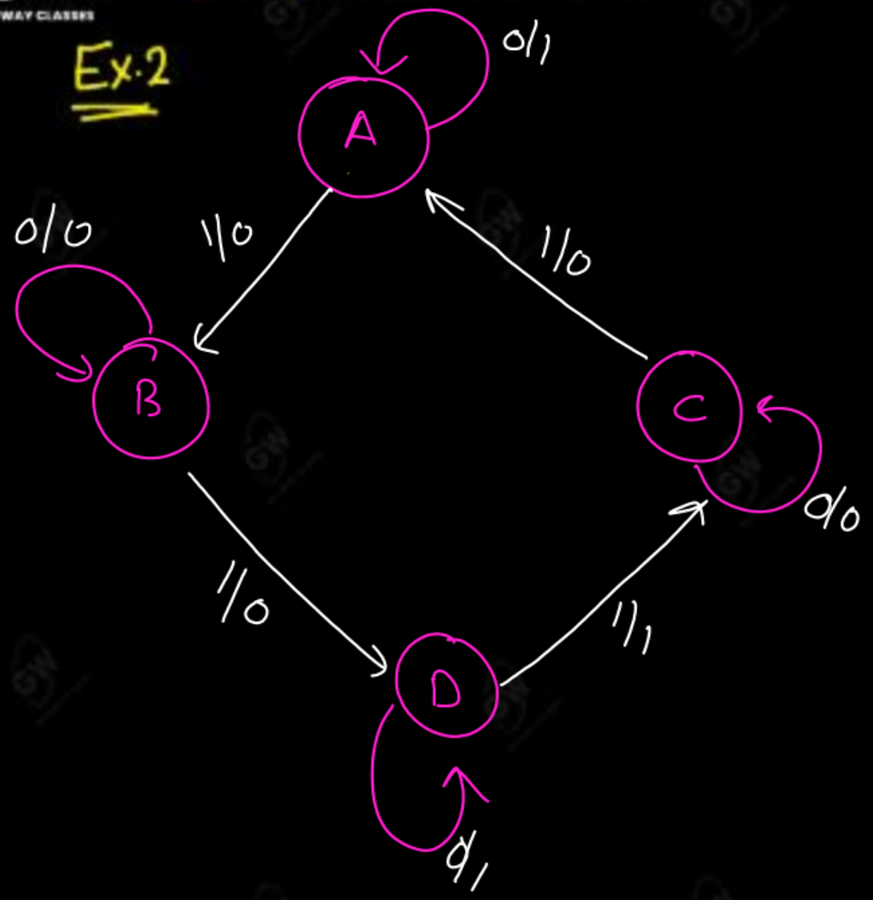
X



Gateway Classes

Design Procedure of Circuit

Ex.2



State table

P.S.	N.S		output	
	x=0	x=1	x=0	x=1
A	A	B	1	0
B	B	D	0	0
C	C	A	0	0
D	D	C	1	1

4 state

$2^n = 4$

$n = 2$

let A = 00
B = 01
C = 10
D = 11

Gateway Classes

Design Procedure of Circuit

J-K

Ex.2

	P.S		I/P	Next state		I/P for ff			
	Q_A	Q_B	X	Q_{A+1}	Q_{B+1}	J_A	K_A	J_B	K_B
A	0	0	0	0	0 0	0	X	0	X
	0	0	1	0	1 1	0	X	1	X
B	0	1	0	0	1 2	0	X	X	0
	0	1	1	1	1 3	1	X	X	0
C	1	0	0	1	0 4	X	0	0	X
	1	0	1	0	0 5	X	1	0	X
D	1	1	0	1	1 6	X	0	X	0
	1	1	1	1	0 7	X	0	X	1

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J_A

Q_A \ Q_BX	00	01	10	11
0			1	
1	X	X	X	X

$J_A = Q_B\bar{X}$

K_A

Q_A \ Q_BX	00	01	11	10
0	X 0	X 1	X 3	X 2
1	1 4	5	7	6

$K_A = \bar{Q}_B X$

J_B

Q_A \ Q_BX	00	01	11	10
0		1	X	X
1			X	X

$J_B = \bar{Q}_A X$

K_B

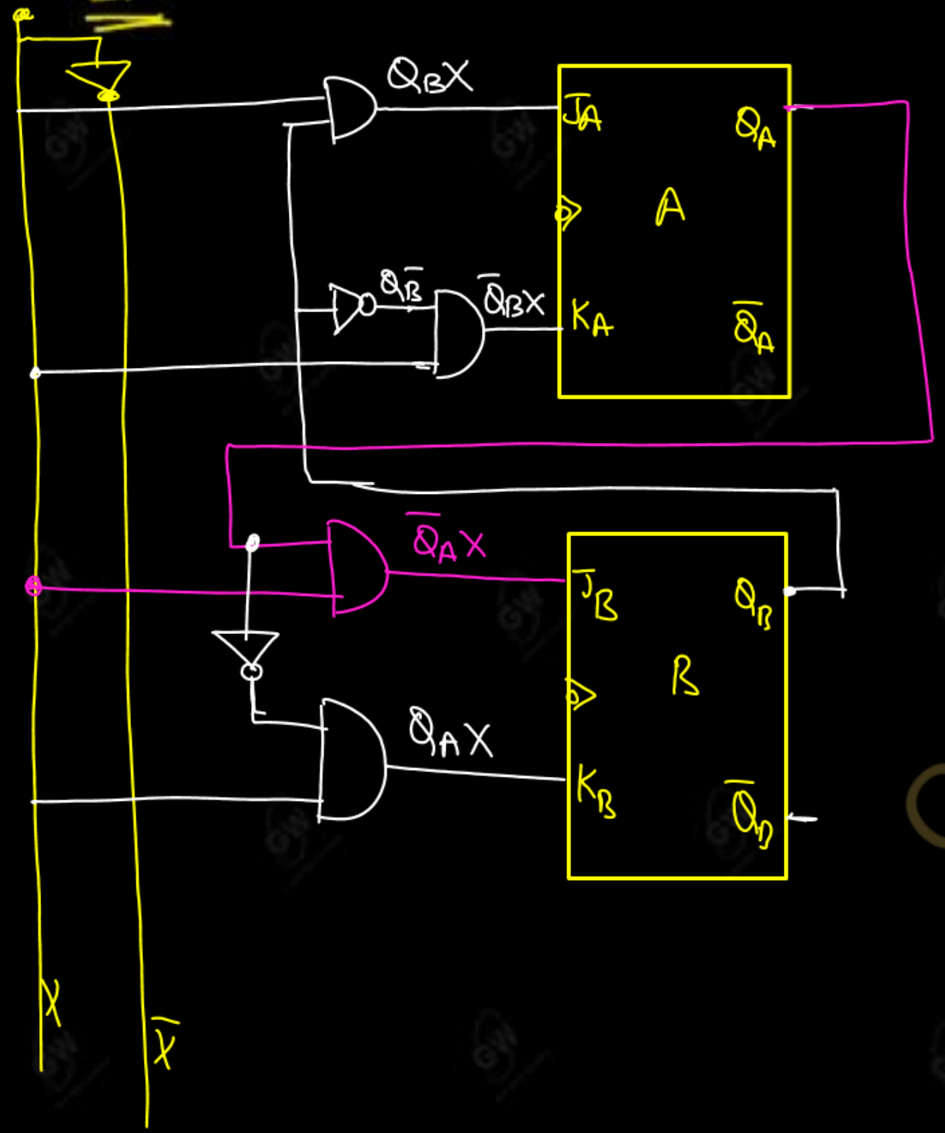
Q_A \ Q_BX	00	01	11	10
0	X	X		
1	X	X	1	

$K_B = Q_A X$

Gateway Classes

Design Procedure of Circuit

Ex.2



$J_A = Q_B X$

$K_A = \bar{Q}_B X$

$J_B = \bar{Q}_A X$

$K_B = Q_A X$

Gateway Classes

Analysis of Clocked Sequential Circuits

The analysis of sequential circuit consists of obtaining a table or a diagram for the time sequence of inputs, outputs and internal states.

Ex 1. Construct the transition table, state table and state diagram for the Moore sequential circuit

1. Determine the flip-flop input equations and the output equations from the sequential circuit.

$$Z = x Q$$

$$T = x Q + \bar{x} \bar{Q}$$

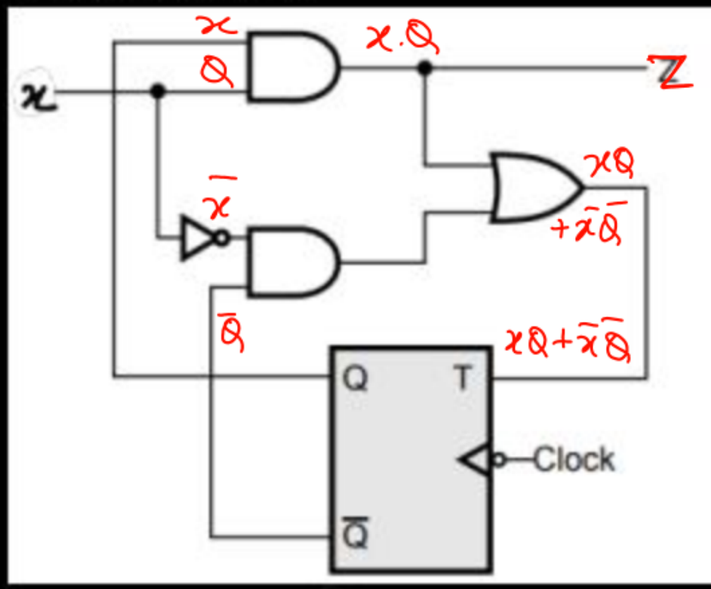
2. Derive the transition equation.

$$Q^+ = T \oplus Q$$

$$Q^+ = (x Q + \bar{x} \bar{Q}) \oplus Q$$

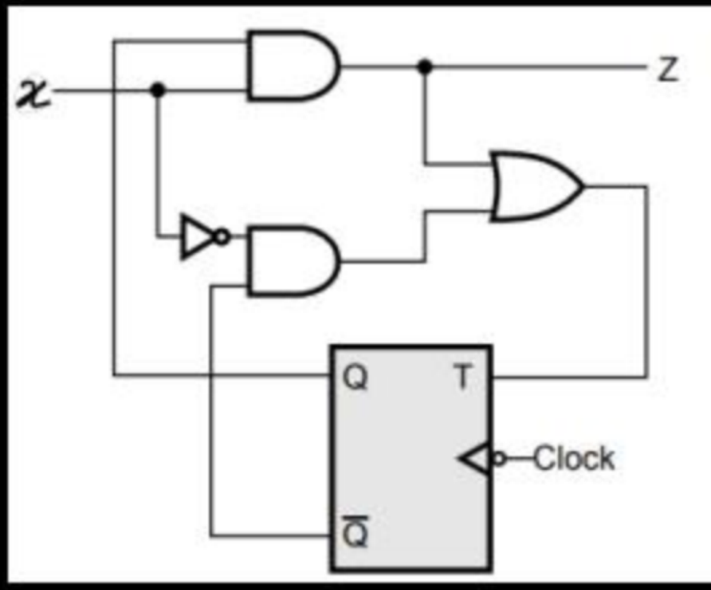
3. Plot the next step map for each flip-flop

$$Q^+ = (x Q + \bar{x} \bar{Q}) \oplus Q$$



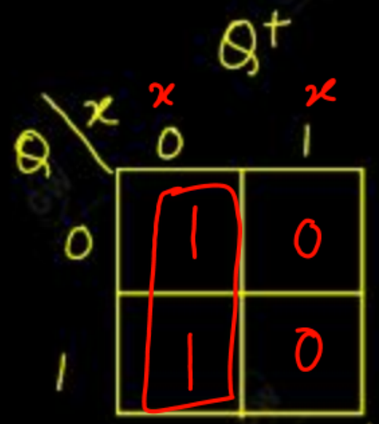
Gateway Classes

Analysis of Clocked Sequential Circuits



4. Plot the transition table

Present state	Next state		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
Q	Q^+	Q^+	Z	Z
$Q=0$	1	0	0	0
$Q=1$	1	0	0	1



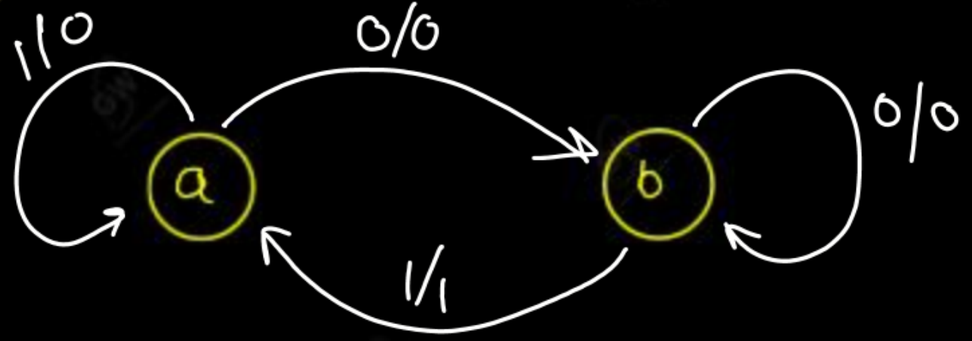
$Q^+ = \bar{x}$

5. Draw the state table $1 \rightarrow b$, $0 \rightarrow a$ $a=0, b=1$

Transition table can be converted into state table. Here, new symbols to binary codes are assigned. a = 0, b = 1.

Present state	Next state		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
a(0)	b	a	0	0
b(1)	b	a	0	1

6. Draw State Diagram



Gateway Classes

Analysis of Clocked Sequential Circuits

Ex 2. Construct the transition table, state table and state diagram for the Moore sequential circuit

1. Determine the flip-flop input equations and the output equations from the sequential circuit.

$F = A \oplus B$ ✓

$J_A = B$, $K_A = \bar{X}B$

$J_B = \bar{X}$, $K_B = X \oplus A$

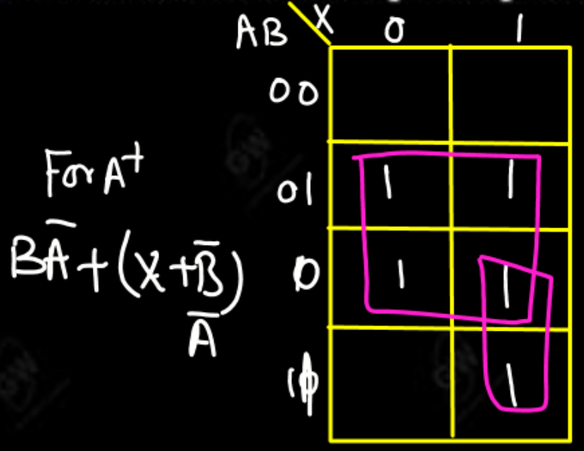
2. Derive the transition equation.

$Q^+ = J\bar{Q} + \bar{K}Q$ → Q.E.

So $A^+ = Q_A^+ = J_A\bar{Q}_A + \bar{K}_A Q_A = B\bar{Q}_A + \overline{\bar{X}B}Q_A = B\bar{Q}_A + (X+\bar{B})Q_A = B\bar{A} + (X+\bar{B})A$

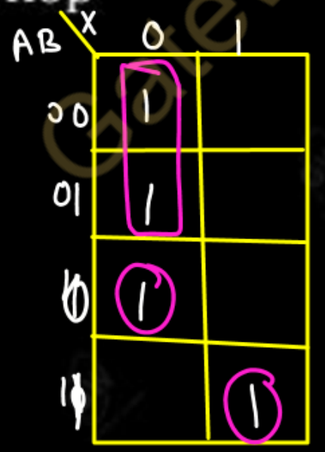
& $B^+ = Q_B^+ = J_B\bar{Q}_B + \bar{K}_B Q_B = \bar{X}\bar{Q}_B + \overline{(X\oplus A)}\cdot Q_B = \bar{X}\bar{B} + (X\oplus A)\cdot B$

3. Plot the next step map for each flip-flop



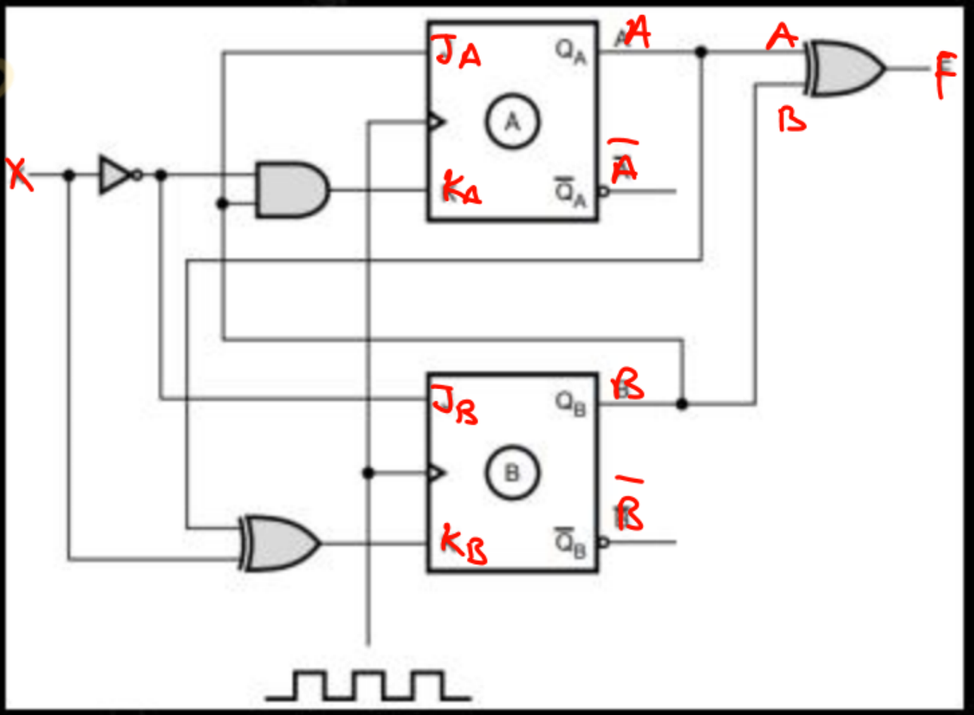
For A^+

$B\bar{A} + (X+\bar{B})\bar{A}$



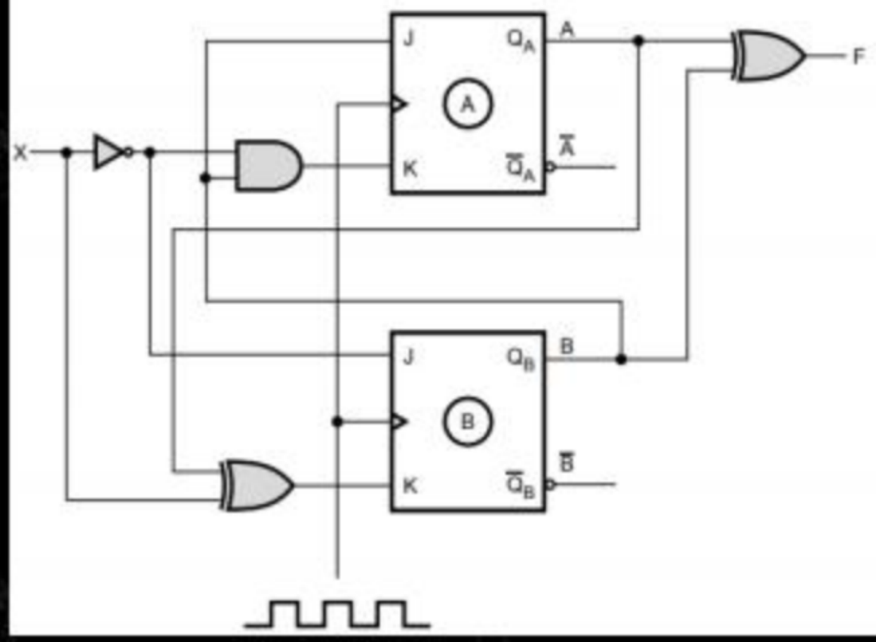
For B^+

$\bar{X}\bar{B} + \overline{(X\oplus A)}\cdot B$



Gateway Classes

Analysis of Clocked Sequential Circuits



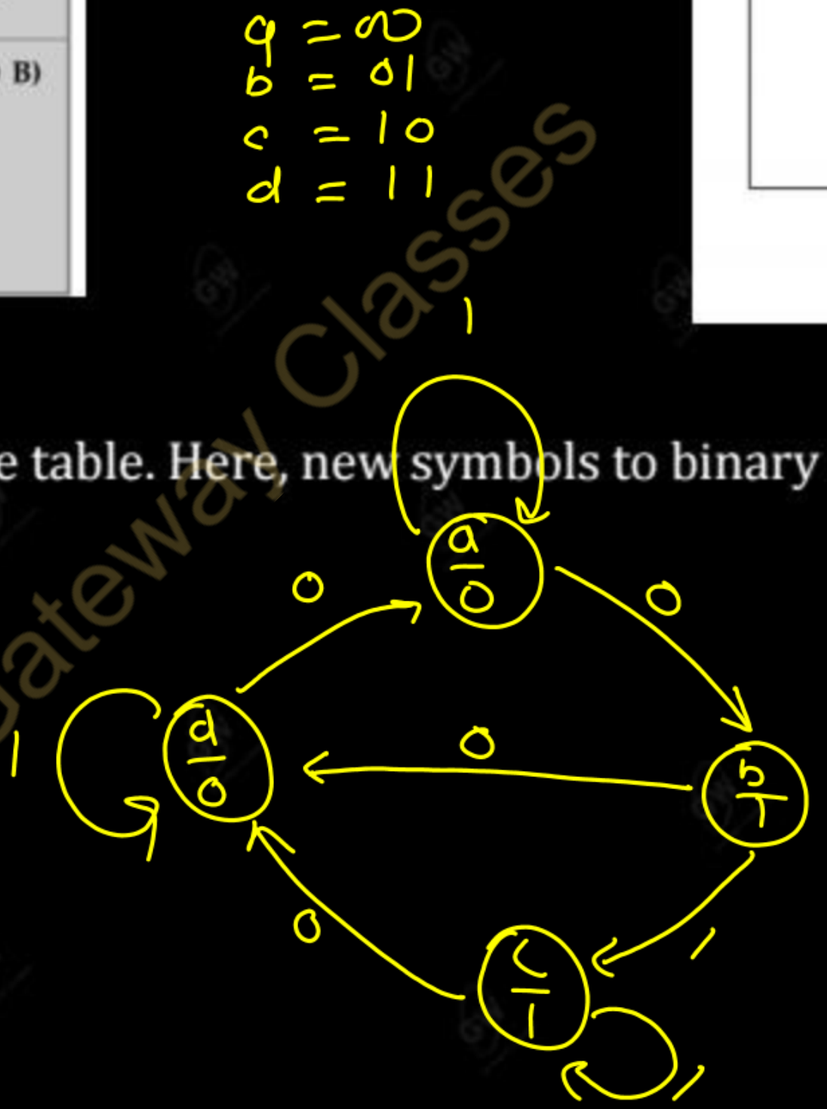
4. Plot the transition table

Present state		Next state				Output
		X = 0		X = 1		
A	B	A^+	B^+	A^+	B^+	F = (A ⊕ B)
0	0	0	1	0	0	0
0	1	1	1	1	0	1
1	0	1	1	1	0	1
1	1	0	0	1	1	0

5. Draw the state table

Transition table can be converted into state table. Here, new symbols to binary codes are assigned

Present state	Next state		Output
A B	X = 0	X = 1	F
	A^+B^+	A^+B^+	
a	b	a	0
b	d	c	1
c	d	c	1
d	a	d	0



In case of Moore model, the directed lines are labelled

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Thank You

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