A K T U

B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-5

Gateway Classes



Avinash Sir

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT- 5

- Digital-to-Analog converters (DAC): Specifications of DACs, Weighted resistor, R2R ladder
- Analog-to-digital converters (ADC): Specifications of ADCs, principle of ADC,
- switched capacitor circuits: Basic concept, practical configurations, ADC etc.
- ADC Types: dual slope, successive approximation, counting type, flash etc

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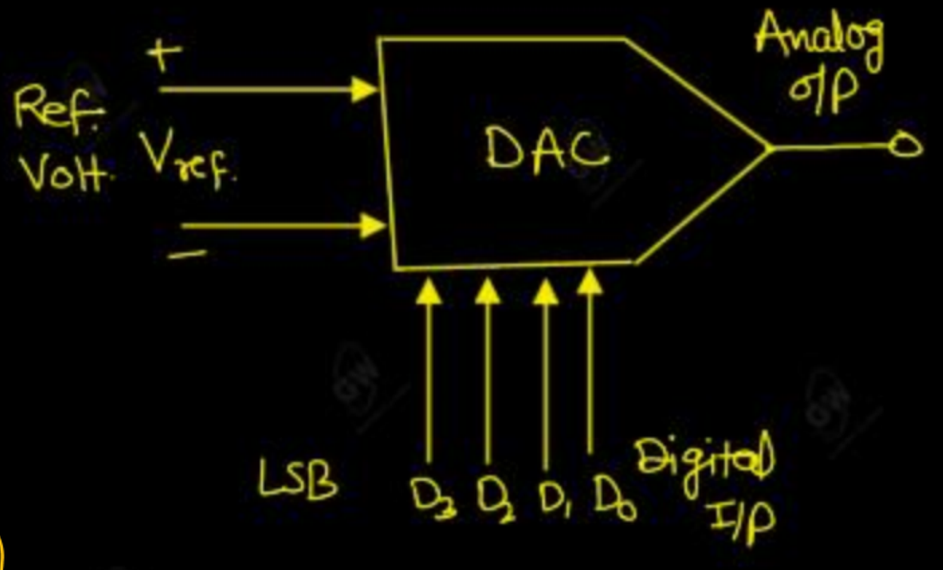
Digital-to-Analog converters (DAC)

A Digital to Analog Converter (DAC) converts a digital input signal into an analog output signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1. DAC consists a number of binary inputs and a single output.

1. Performance Parameters of DAC

a) Accuracy:- It is a comparison of actual output voltage with expected output. It is expressed in percentage. Ideally, the accuracy of DAC should be, at worst, ± 1/2 its LSB. If the full scale output voltage is 10.2 V then for an 8-bit DAC accuracy can be given as

$$\text{Accuracy} = V_{oFS} / (2^n - 1).2 = 10.2 / (255 \times 2) = 20\text{mV}$$



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Digital-to-Analog converters (DAC)

b. Resolution:- Resolution is defined in two ways.

- Resolution is the number of different analog output values that can be provided by a DAC. For an n-bit DAC, *Resolution = 2^n*
- Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs. For an n-bit DAC it can be given as , *Resolution = $V_{oFS} / 2^n - 1$*

where, V_{oFS} = Full scale output voltage

For an 8-bit DAC resolution can be given as

Resolution = $2^n = 2^8 = 256$

If the full scale output voltage is 10.2 V then by second definition the resolution for an 8-bit DAC can be given as

$$\text{Resolution} = \frac{V_{ofs}}{2^n - 1} = \frac{10.2}{2^8 - 1} = \frac{10.2}{255}$$

$$= 40 \text{ mV / LSB}$$

Therefore, we can say that an input change of 1 LSB causes the output to change by 40 mV.

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c. Conversion Time:- It is a time required for conversion of analog signal into its digital equivalent. It is also called setting time. It depends on the response time of the switches and the output of the amplifier.

d. Settling Time:- This is the time required for the output of the DAC to settle to within ±1/2 LSB of the final value for a given digital input i.e. zero to full scale.

e. Stability:- The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges. These parameters represent the stability of the converter.

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Digital-to-Analog converters (DAC)

Ex.1 *Determine the output voltage produced by a 4-bit DAC whose output voltage range is 0 to 10 V when the input binary number is 0110.*

$n=4$, $V_{FS} = 10\ V$

0 1 1 0

Solution : Given VoFS = 10 V

Resolution = $10 / 2^4 - 1 = 0.6667$ V

$\frac{10}{2^4-1}$

The output voltage at 0110 = $0.6667 \times 6 = 4$ V

↳ Decimal 6

Ex.2 *An 8-bit DAC has resolution of 20 mV/LSB. Find VoFS and Vo if the input is (10000000)2.*

$2^8 \leftarrow 2^2 2^1 2^0$

Deci

128

Solution :

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1}$$

$$20m = \frac{V_{OFS}}{2^8 - 1} = \frac{V_{OFS}}{255}$$

$$V_{OFS} = 255 \times 20 \times 10^{-3} = 5.1 \text{ Volt}$$

D = equivalent of $(10000000)_2 = 128$

$V_o = \text{Resolution} \times D = 20 \times 128 = 2.56$ V Ans.

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Digital-to-Analog converters (DAC)

0.06 × 100 = 6°C

Input and output Equations



Analog output V_o = K × digital Input

where K = Scaling factor

$$V_o = V_{FS}\left[d_1 2^{-1} + d_2 2^{-2} \cdots\cdots d_n 2^{-n}\right]$$

where d_1 = MSB , d_n = LSB

let us put $V_{FS} = K V_R$

$$V_o = K V_R \left[d_1 2^{-1} + d_2 2^{-2} + \cdots d_n 2^{-n}\right]$$

Ex: find Analog o/p for 4 bit DAC if Digital I/P is 1011 . Assume $V_{FS} = 5V$

Sol:

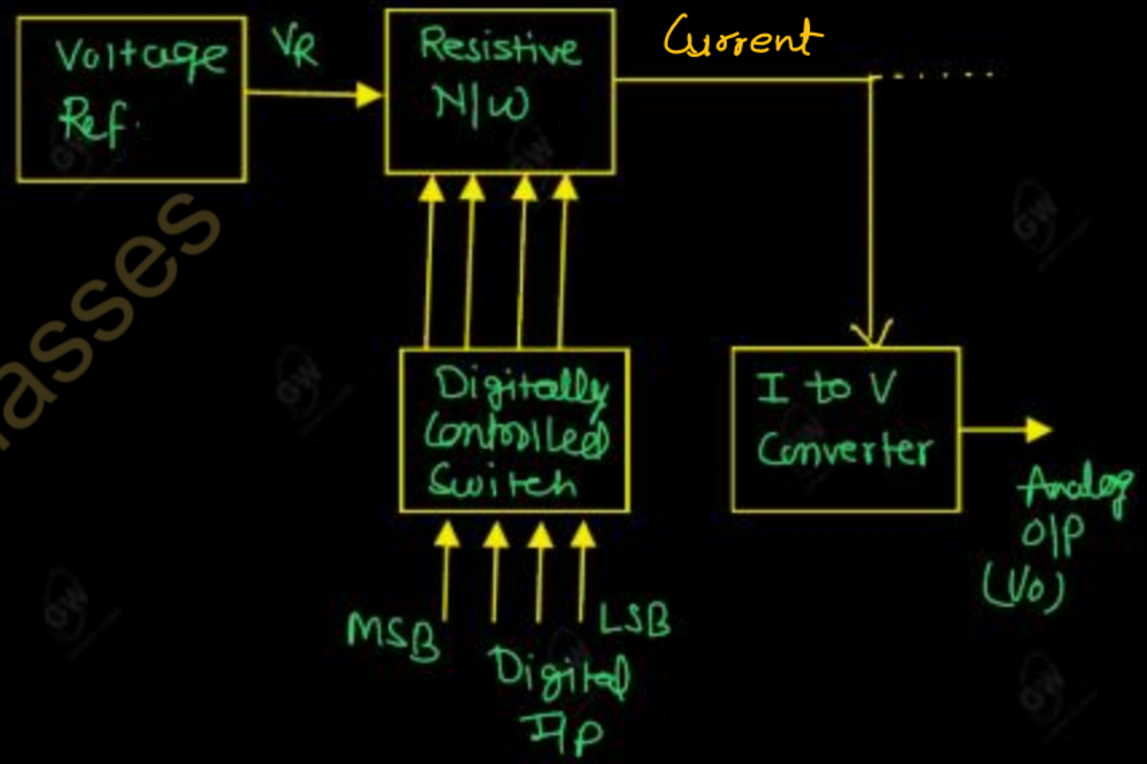
$$V_o = 5\left[1\times2^{-1} + 0\times2^{-2} + 1\times2^{-3} + 1\times2^{-4}\right] = 5\left[\frac{1}{2} + 0 + \frac{1}{8} + \frac{1}{16}\right]$$

$V_o = 3.4375$ Volt Ans

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Digital-to-Analog converters (DAC)

- The basic building blocks of a DAC are a *resistive network, digitally controlled electronic switches, a voltage reference, and a current-to-voltage converter.*
- A digital input code is applied to the resistive network via the digitally controlled switches. The digitally controlled switches are turned on or off by the digital input bits (0's and 1's)



- The output of the resistive network is in the form of current. It can be converted into a proportional voltage with the help of a current-to-voltage converter. Thus, we obtain an analog output voltage proportional to the digital input code.
- The actual digital-to-analog conversion takes place within the resistive network.

Gateway Classes

Types of D/A Converter

There are mainly two techniques used for analog to digital conversion

- Binary weighted resistor D/A converter
- R/2R ladder D/A converter

In these techniques, the shunt resistors are used to generate n binary weighted currents. These currents are added according to switch positions controlled by the digital input and then converted into voltage to give analog voltage equivalent to the digital input. Therefore, such digital to analog converters are called current driven DACs.

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• Binary weighted resistor D/A converter

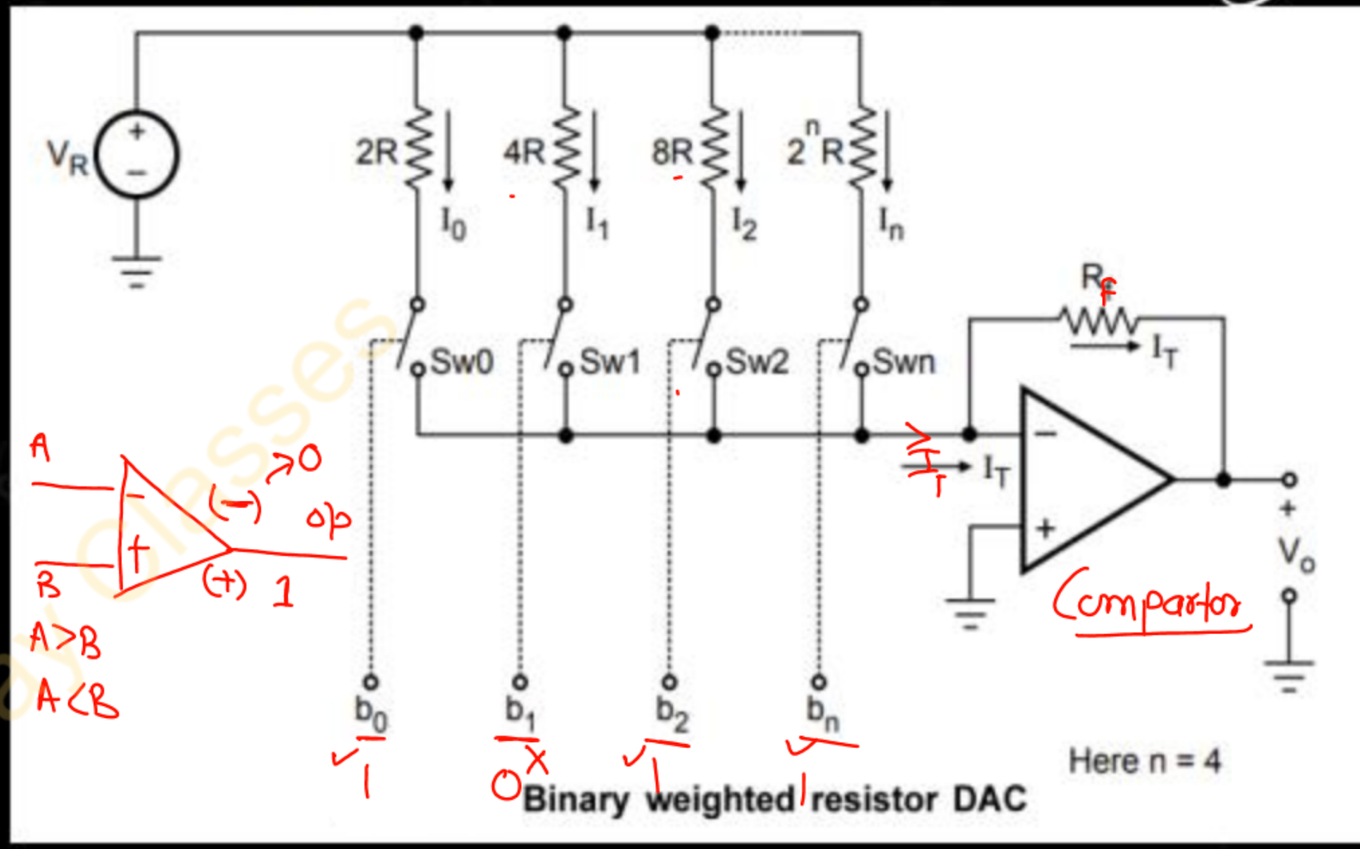
The binary weighted resistor DAC uses an op-amp to sum n binary weighted currents derived from a reference voltage VR via current scaling resistors 2R, 4R, 8R, ..., 2n R,

switch positions are controlled by the digital inputs. When digital input is logic 1, it connects the corresponding resistance to the reference voltage VR; otherwise it leaves resistor open. Therefore,

For ON-switch, I = VR / R and

For OFF-switch, I = 0

Here, operational amplifier is used as a summing amplifier. Due to high input impedance of op-amp, summing current will flow through Rf.



Binary weighted resistor DAC

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• Binary weighted resistor D/A converter

➤ Hence the total current through Rf can be given as

$$I_T = I_0 + I_1 + I_2 + \dots + I_n$$

➤ The output voltage is the voltage across R_f and it is given as

$$V_o = -I_T \cdot R_f = -R_f\left(b_0\frac{V_R}{2R} + b_1\frac{V_R}{4R} + b_2\frac{V_R}{8R} + \cdots\right)$$

$$V_o = -V_R \cdot \frac{R_f}{R}\left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} - \cdots\right]$$

if $R_f = R$ then

$$V_o = -V_R\left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots\right] = b_0 2^{-1} + b_0 2^{-2}$$

Ex. find o/p voltage for a 4 bit Input 1010 with $R_f = R$ & $V_f = 5V$

Sol:

$$V_o = -5\left[\tfrac{1}{2}\times 1 + 0\times\tfrac{1}{4} + 1\times\tfrac{1}{8} + 0\times\tfrac{1}{16}\right] = -5\left[\tfrac{1}{2} + \tfrac{1}{8}\right]$$

$$= -3.125 \text{ volt}$$

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• Binary weighted resistor D/A converter

Drawbacks :

1. Wide range of resistor values are required. For 8-bit DAC, the resistors required are 2^1 R, 2^2 R, 2^3 R,... and 2^8 R. Therefore, the largest resistor is 128 times the smallest one.

2. This wide range of resistor values has restrictions on both, higher and lower ends. It is impracticable to fabricate large values of resistor in IC, and voltage drop across such a large resistor due to the bias current also affects the accuracy. For smaller values of resistors, the loading effect may occur.

3. The finite resistance of the switches disturbs the binary-weighted relationship among the various currents, particularly in the most significant bit positions, where the current setting resistances are smaller.

All these drawbacks, especially the requirement of wide range of resistors restricts the use of binary weighted resistor DACs below 8-bits.

Gateway Classes

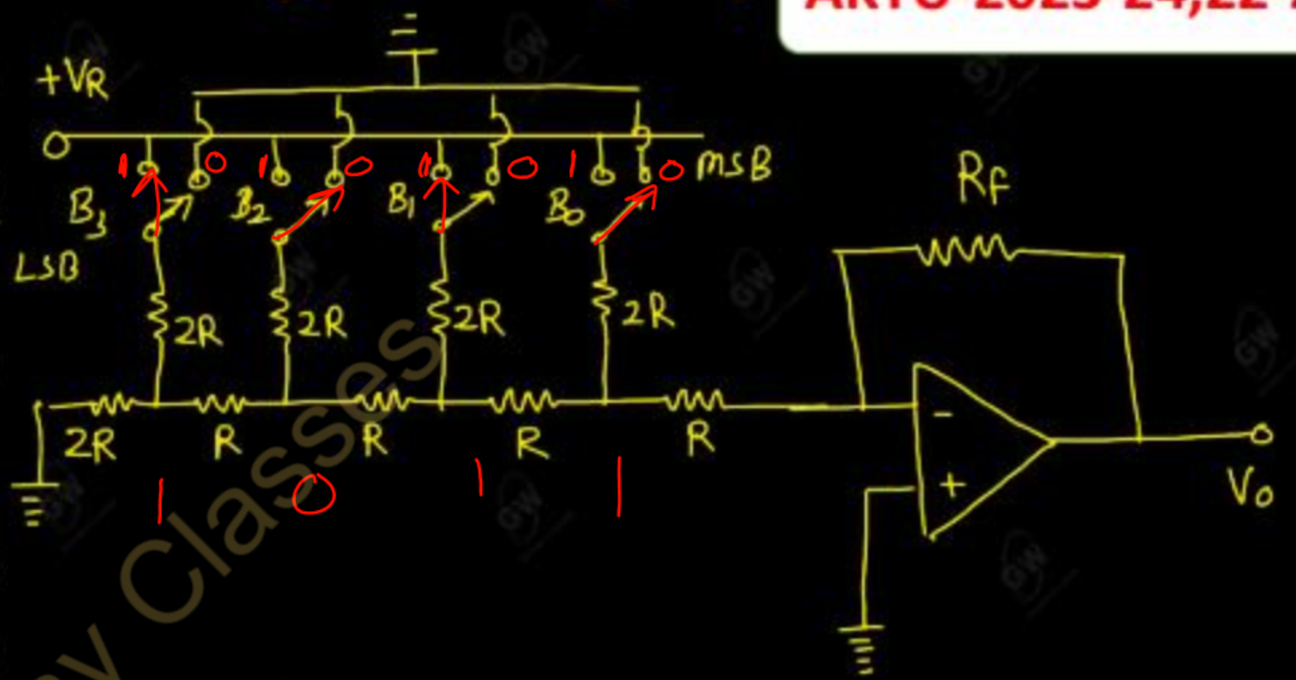
R-2R Ladder Digital to Analog Converter (DAC)

AKTU-2023-24,22-23

R- 2R ladder circuit is made by adding combination R & 2R resistor in cascaded form as shown in the following figure.

There are only two types of resistors used. Each stage contains R & 2R, is used for a single bit.

There is switch between the Vref & GND which is controlled by the binary input. Bit 0 means the GND is connected & bit 1 means the Vref is connected.



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R-2R Ladder Digital to Analog Converter (DAC)

Working:-

Equivalent resistance is always R

$$V_o = -\frac{R_f}{R}\left[\frac{1}{2}B_0 + \frac{1}{4}B_1 + \frac{1}{8}B_2 + \cdots\right]V_R$$

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Advantages of R-2R Ladder DAC;

- Uses only two types of resistors
- Easily scalable to any number of bits
- Output impedance is always R

R-2R Ladder Digital to Analog Converter (DAC)

Example1 Design a 4 bit R-2R ladder network, determine the size of each step if R = 10 kΩ, Rf = 20 kΩ and VCC = ± 15 V. Calculate the output voltage for Do = 1, D1 = 0, D2 = 1 and D3 = 1 if bit '1' applied as 5 V and bit 'O' applied as 0 V.

$$V_o = \frac{V_R \times 20\,K}{10\,K}\left(D_3\,2^{-1} + D_2\,2^{-2} + D_1\,2^{-3} + D_0\,2^{-4}\right)$$

$$V_{OFS} = \frac{V_R \times 20\,K}{10\,K}\left(1\times2^{-1} + 1\times2^{-2} + 1\times2^{-3} + 1\times2^{-4}\right)$$

$$= 5 \times 2\,(0.9375)$$

$$= \mathbf{9.375\ V}$$

$$\text{Resolution} = \text{Size of each step} = \frac{V_{OFS}}{2^n - 1} = \frac{9.375}{2^4 - 1} = \mathbf{0.625\ V}$$

Output voltage for : $D_0 = 1$, $D_1 = 0$, $D_2 = 1$ and $D_3 = 1$

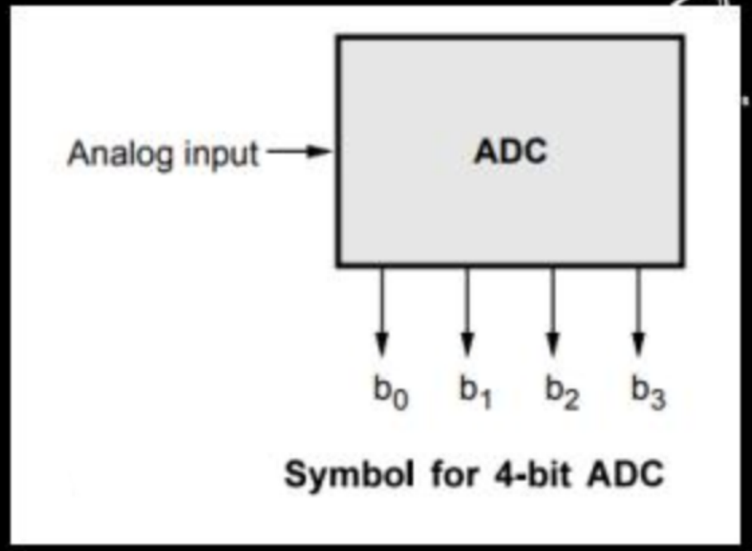
$$V_o = \text{Resolution} \times D \qquad \text{where D = Decimal of (1101) = 13}$$

$$= 0.625 \times 13$$

$$= \mathbf{8.125\ V}$$

Gateway Classes

ADC (Analog to Digital Converter)



Symbol for 4-bit ADC

The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word. Thus the A/D converter is exactly opposite function that of the D/A converter.

Performance Parameters of ADC

a. Resolution:- ADC resolution is the same as for 8 the DAC and is repeated here :

$$\text{Resolution} = 2^n$$

Resolution is also defined as the ratio of a change in value of input voltage, V,-, needed to change the digital output by 1 LSB. If the full scale input voltage required to cause a digital output of all l's is ViFS, then resolution can be given as

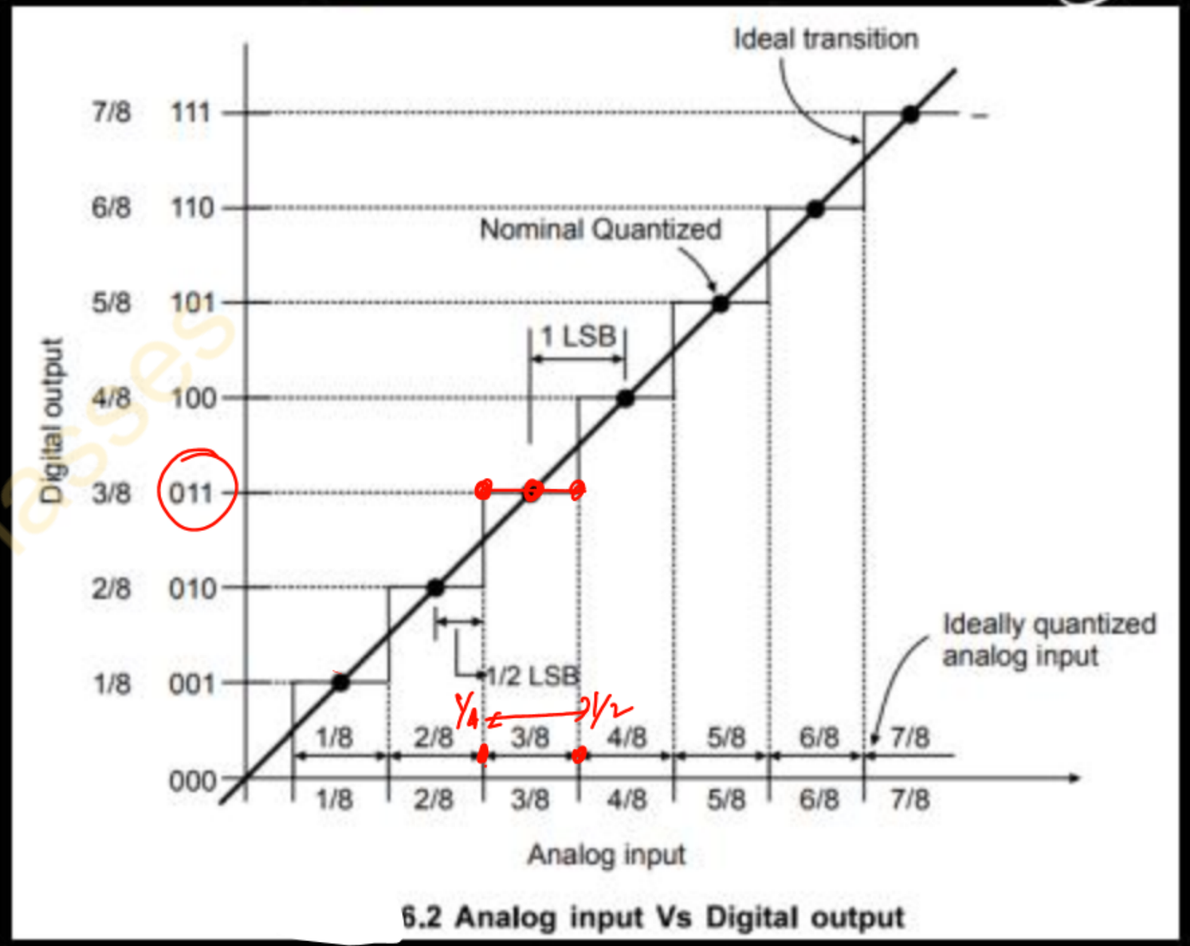
Gateway Classes

ADC (Analog to Digital Converter)

b. Quantization Error:-

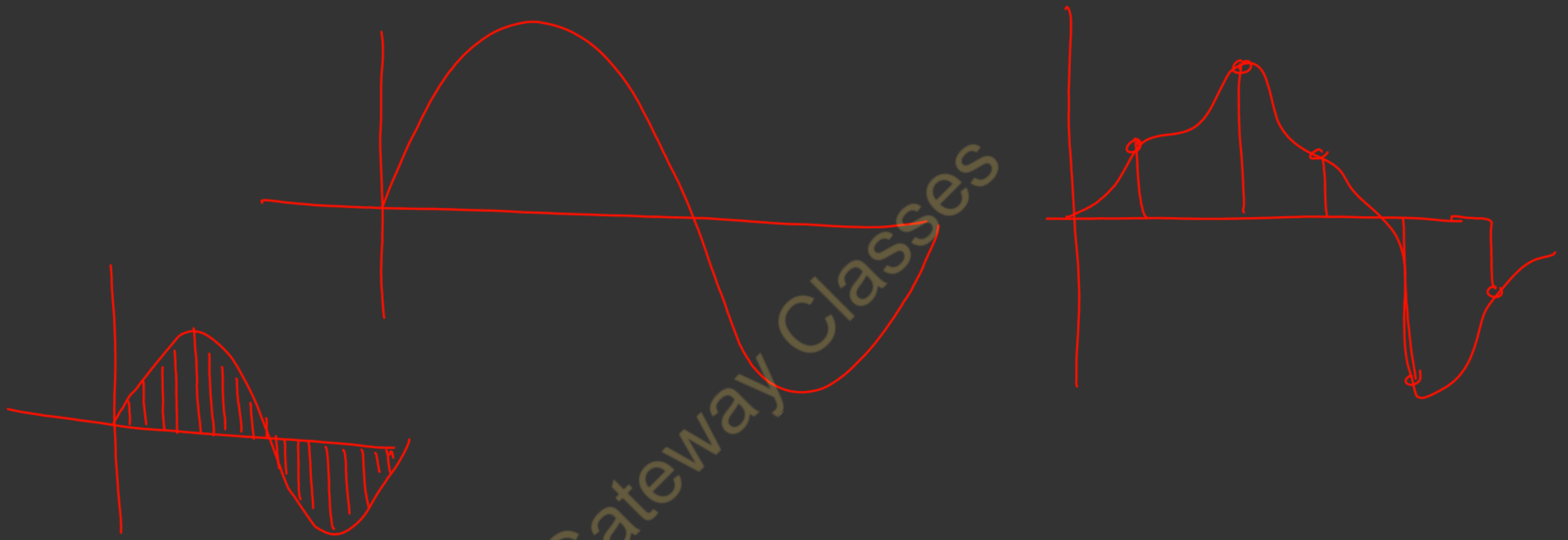
Fig. shows that the binary output is 011 for all values of Vi between 1/4 and 1/2 Vi. There is an unavoidable uncertainty about the exact value of Vi when the output is 011 This uncertainty is specified as quantization error. Its value is ± 1/2 LSB.

It is given as, QE = V_{iFS} /2.(2^n – 1) Increasing the number of bits results in a finer resolution and a smaller quantization error.



6.2 Analog input Vs Digital output

Gateway Classes



Gateway Classes

ADC (Analog to Digital Converter)

C. Accuracy :-Absolute accuracy is the maximum deviation between the actual ADC output and the ideal ADC output. The relative accuracy is the maximum deviation after gain and offset errors have been removed.

d. Linearity:- It is an important parameter of the accuracy of ADC. It indicates how close the ADC output is to its ideal transfer characteristics.

e. Settling Time:-It is the time taken by the output of ADC to settle within a specified band ±(1/2) LSB of its final value following a code change at the input (generally a full scale change).

f. Specifications of Sample and Hold Circuit:- For accurate analog to digital conversion the analog input voltage should be held constant during the conversion cycle. The sample and hold circuit does this task.

Gateway Classes

ADC (Analog to Digital Converter)

Example 1 An 8-bit ADC outputs all l's when Vi -5.1 V. Find its a) Resolution and b) Digital output when V i - 1.28 V.

Solution : a) Resolution = $2^n = 2^8 = 256$

and resolution = 5.1 V / $(2^8 - 1)$ = 20 mV/LSB

Therefore, we can say that to change output by 1 LSB we have to change input by 20 mV.

b) For 1.28 V analog input, digital output can be calculated as,

D = 1.28 V / 20mV / LSB = 64 LSBs

The binary equivalent of 64 is $(0100\ 0000)_2$

GatewayClasses

ADC (Analog to Digital Converter)

Example 2 Calculate the quantizing error for 12-bit ADC with full scale input voltage 4.095 V.

Solution :

$$Q_E = \frac{V_{FS}}{(2^n - 1)\,2} = \frac{4.095}{(2^{12} - 1) \times 2}$$

$$Q_E = \frac{4.095}{4095 \times 2} = 0.5 \text{ mV}$$

Ans

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ADC (Analog to Digital Converter)

ADCs various conversion techniques :

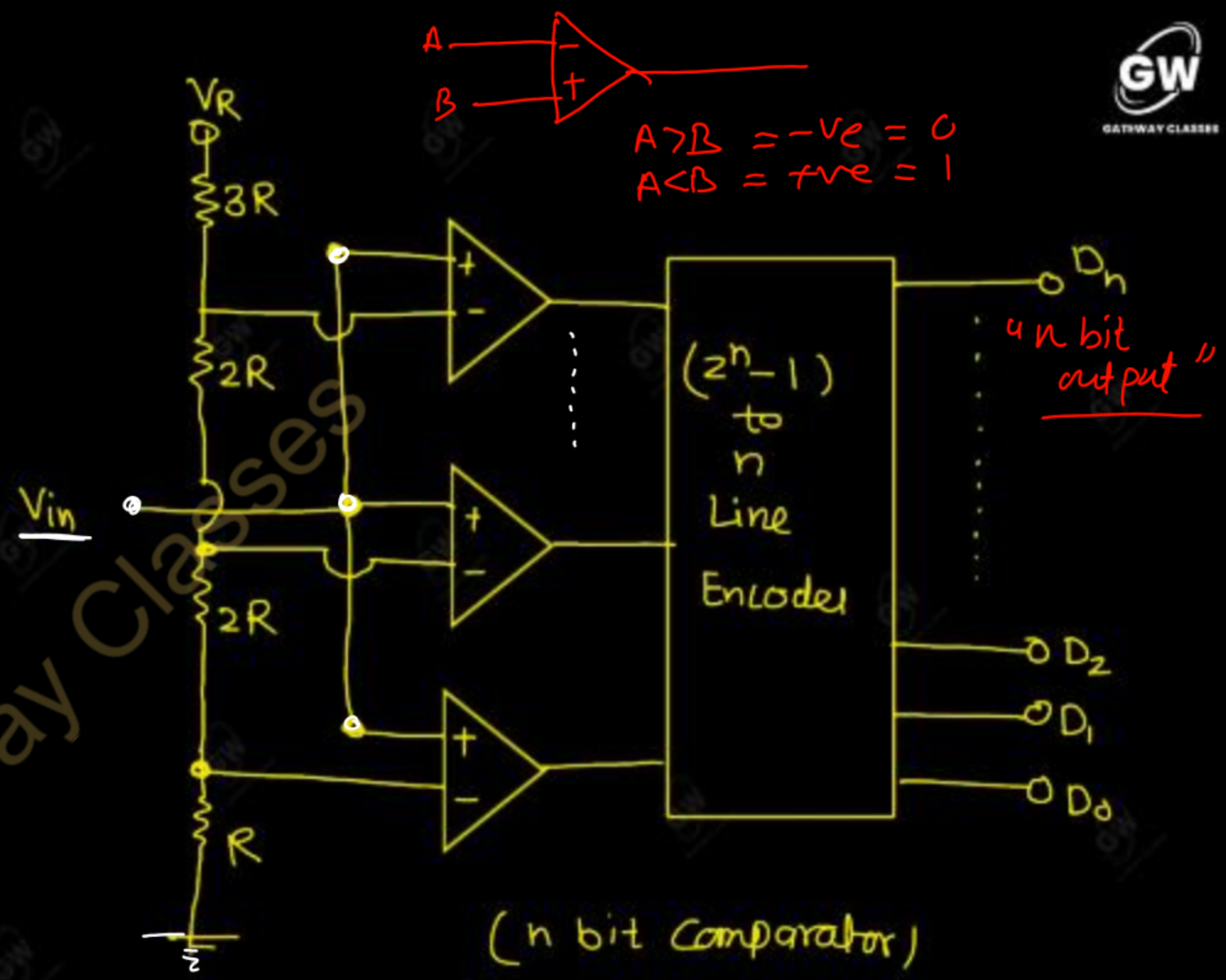
1. Flash type or parallel comparator
2. Successive approximation (SAR)
3. Single ramp or single slope / Counter type
4. Dual slope

Gateway Classes

Flash type or parallel comparator:- The comparators give output "1" or "0" state depending on whether the input signal is above or below the reference level at that instant. Those comparators referred above the input signal, remain turned-off, representing a "0" state. The comparators at or below the input signal conversely become a "1" state. The code resulting from this comparator is converted to a binary code by the encoder

The number of comparators required for n bit resolution is,

Number of comparators = $2^n - 1$

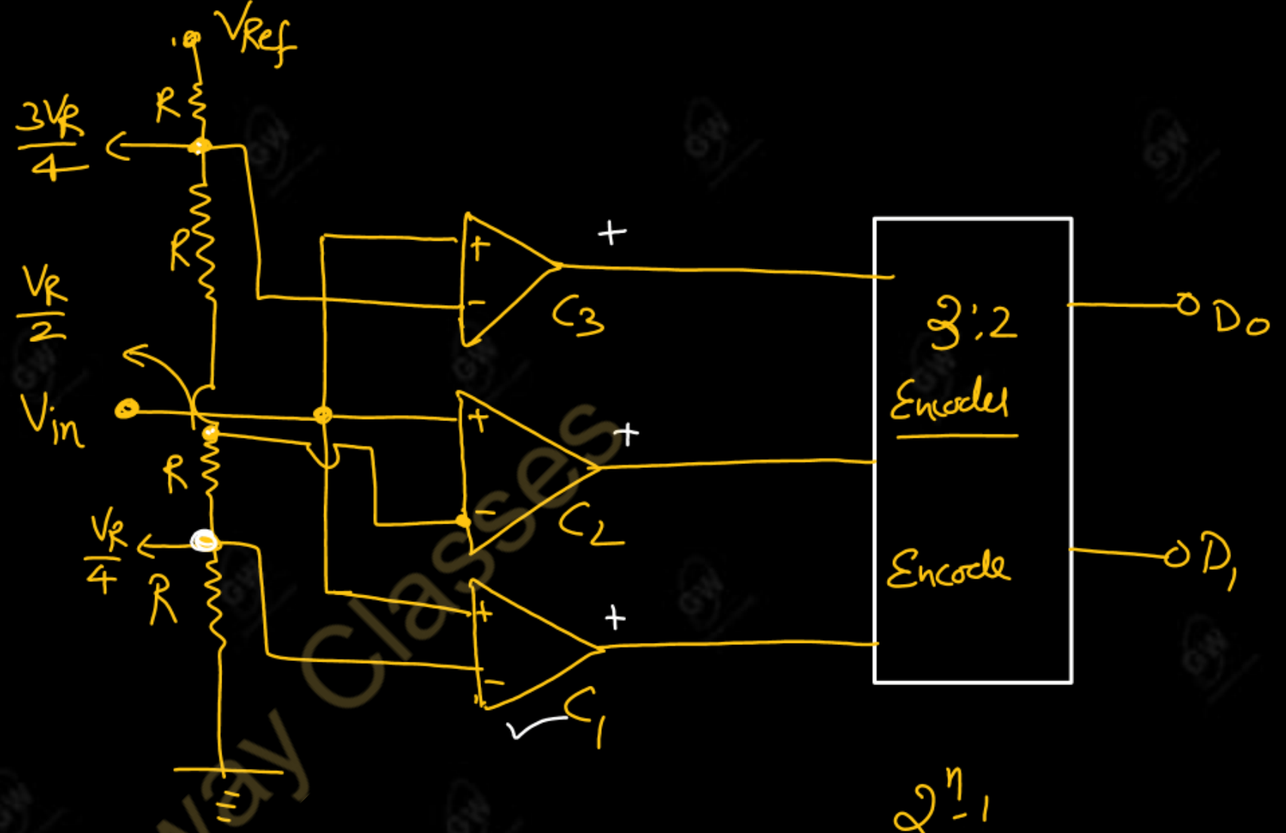


Gateway Classes

2- Bit Comparator

$\frac{V_R}{4} > V_{in}$

V_{in}	C_1	C_2	C_3	D_0	D_1
$< \frac{V_R}{4}$	0	0	0	0	0
$\frac{V_R}{4} < V_{in} < \frac{V_R}{2}$	1	0	0	0	1
$\frac{V_R}{2} < V_{in} < \frac{3V_R}{4}$	1	1	0	1	0
$V_{in} > \frac{3V_R}{4}$	1	1	1	1	1



Case(i) $\frac{V_R}{4} > V_{in}$, the C_1, C_2, C_3 = -Ve

0

Case(ii) $\frac{V_R}{4} < V_{in} < \frac{V_R}{2}$, C_1 = +Ve, 1

C_2 = -Ve 0, C_3 = -Ve 0

$2^n - 1$

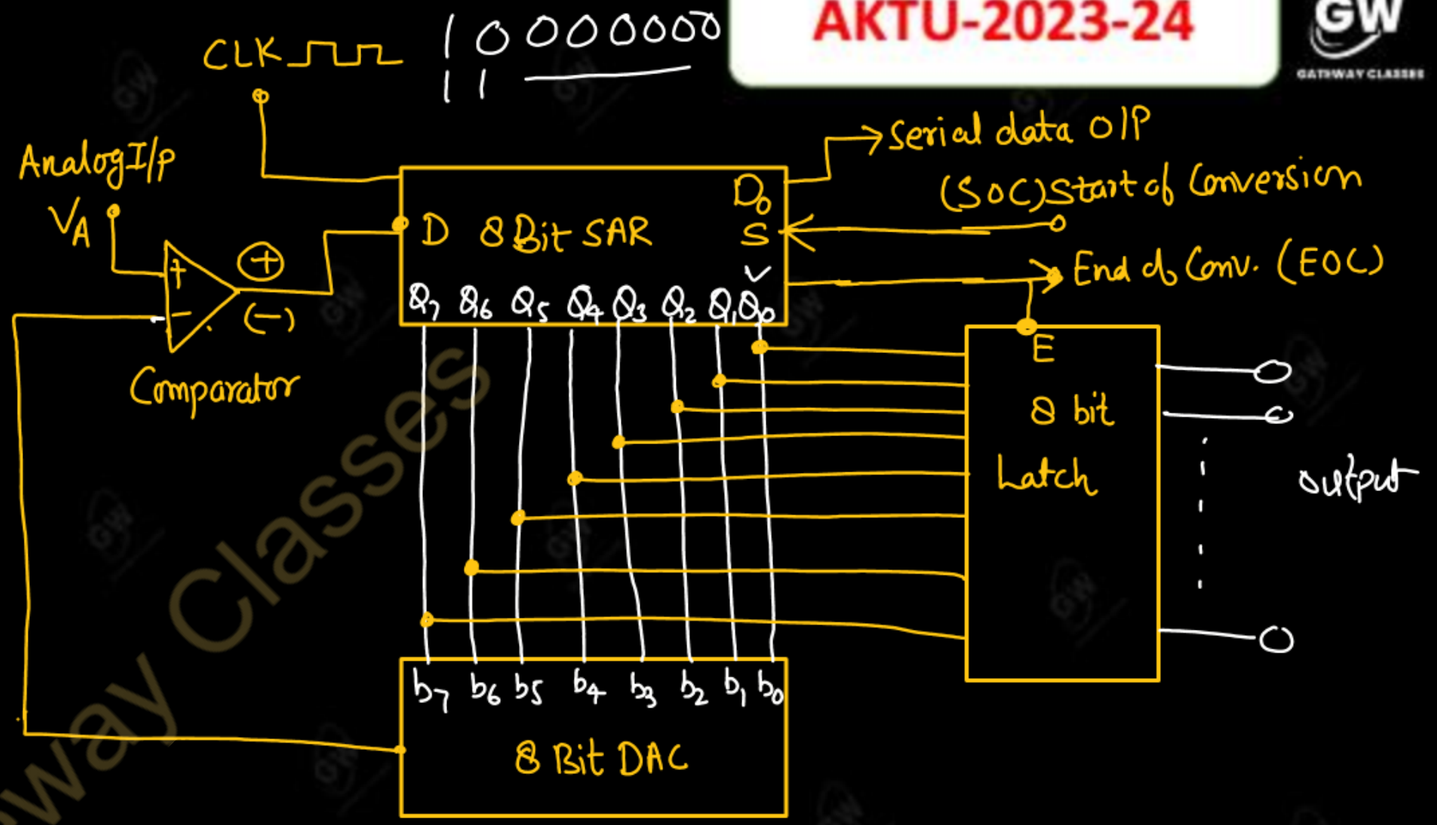
$2^2 - 1 = 3$

Drawback → Size

Gateway Classes

Successive approximation ADC :- In this technique, the basic idea is to adjust the DAC's input code such that its output is within ± 1/ 2 LSB of the analog input Vi to be A/D converted. The code that achieves this represents the desired ADC output.

The successive approximation method uses very efficient code searching strategy called binary search. It completes searching process for n-bit conversion in just n clock periods.



Gateway Classes

15 V

let 15 V = 1111

= 00001111

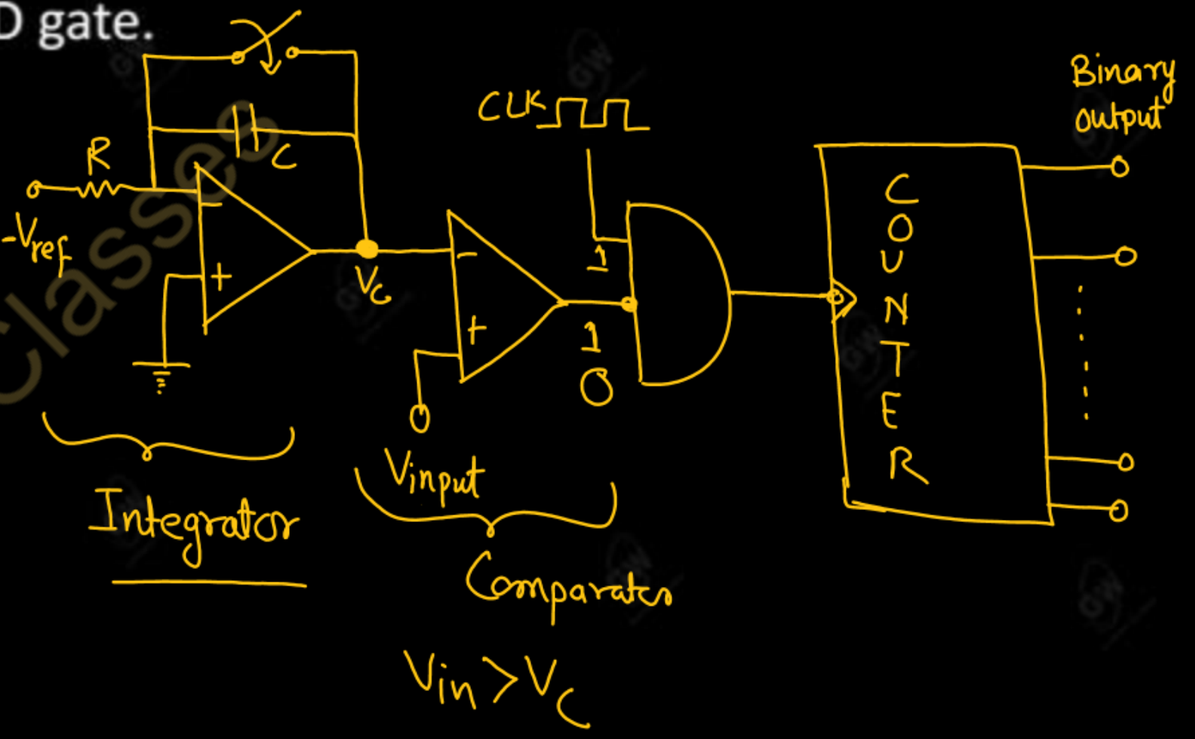
Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	V_0	Comp.	o/p
0	0	0	0	0	0	0	1	1V	+ve	1
0	0	0	0	0	0	1	1	3V	+ve	1
0	0	0	0	0	1	1	1	7V	+ve	1
0	0	0	0	1	1	1	1	15V	+ve	1
0	0	0	X0	1	1	1	1	31	-ve	0
0	0	X0	0	1	1	1	1		-ve	0
0	X0	0	0	1	1	1	1		-ve	0
1	0	0	0	1	1	1	1		-Ve	0

Gateway Classes

Counter type/ Ramp type ADC/Single Slope:- A comparator is used at the input to compare input analog voltage with feedback reference voltage provided by DAC. An up/down counter is used to count the number of clock pulses applied through AND gate.

When conversion started , counter is reset to zero and input analog voltage is applied to terminal of the comparator, when analog voltage is greater than feedback voltage provided by DAC, comparator o/p is logic 1 due to which clock pulses are applied to counter & counter will increase counting.

When analog voltage is less than feedback voltage then o/p of comparator is logic 0 and counter will stop. At this time, o/p of counter will provide binary equivalent of i/p analog voltage.



Gateway Classes

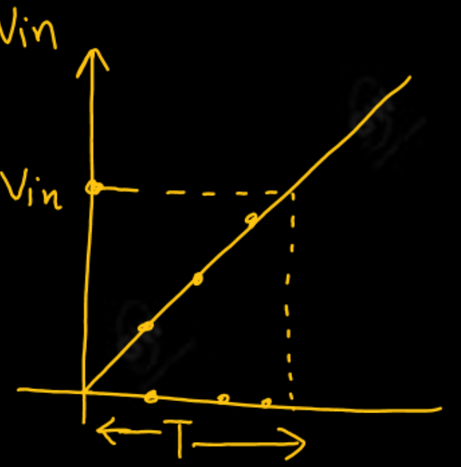
output of integrater is given by

$$V_o = \frac{1}{\tau}\int_0^t V_{in}\, dt$$

where τ = time Constant of RC Circuit

$$V_o = \frac{1}{RC}\int_0^t V_{ref}.\, dt$$

$$\boxed{V_o = \frac{1}{RC} V_{ref}.\, T_1}$$



So output of Comparator is 1 till Capacitor is fully charged upto V_{in}.

⇒ Counter Count Clock pulse & when $V_C = V_{in}$ or greater then output of gate is Zero. After that Counter not Count.

⇒ So Counter stored value upto V_{in}

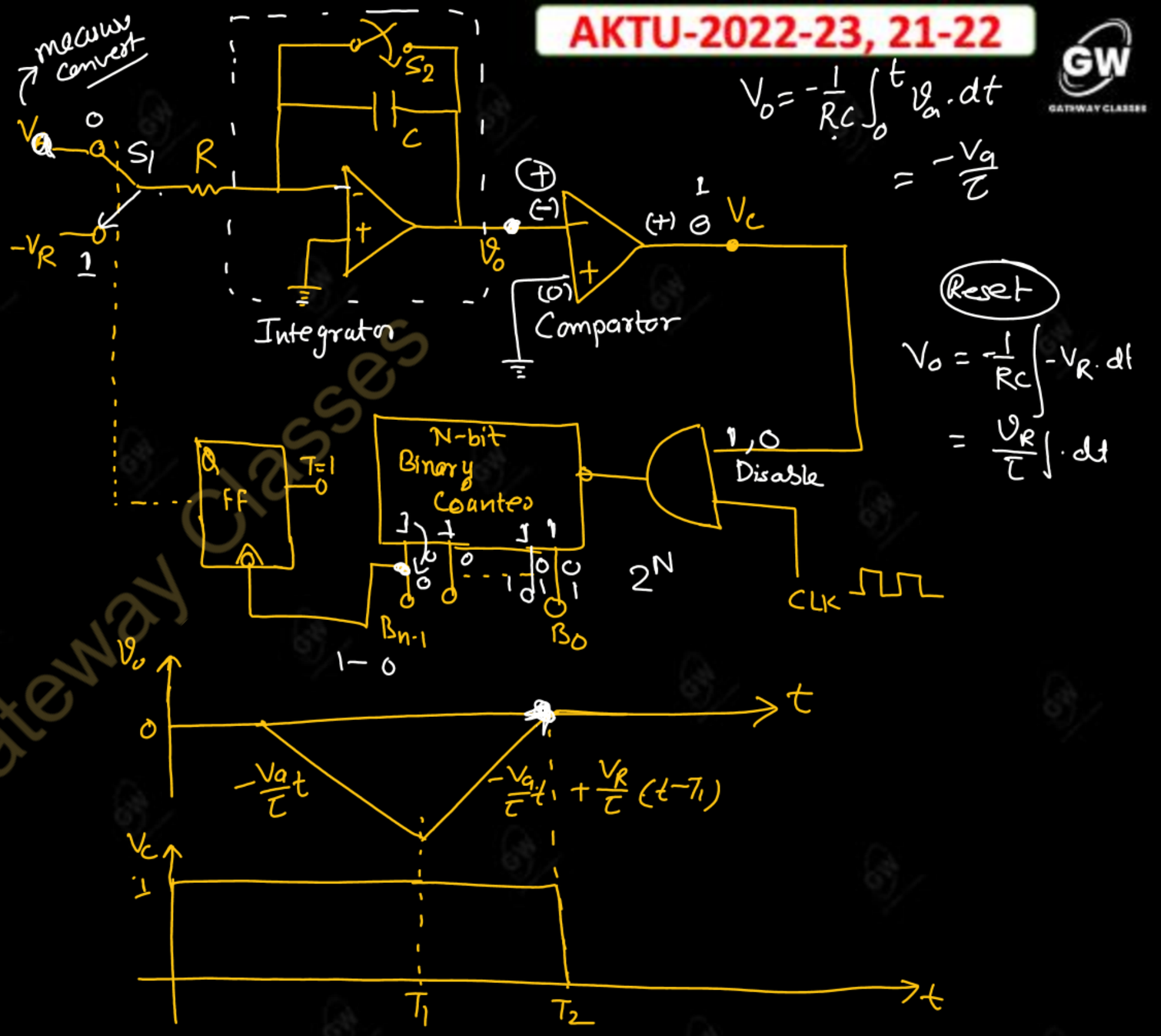
⇒ Switch is closed as Comparter output is zero. Capacitor is short Circuited or reset for next operation.

Gateway Classes

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Dual Slope ADC:-

- It is the most accurate ADC but the slowest one. In this type, an integrator is used to integrate the analog voltage and negative reference voltage.
- When conversion started ,counter and T Flip flop are set to 0 and switch is connected to analog voltage.
- During analog voltage integration, o/p is negative, due to which comparator o/p is logic 1 and counter will continuously increase .



Gateway Classes

Dual Slope ADC:-

- After 2n clock pulse, counter will reach 0 again, at this time T flip flop toggle to 1 and switch become connected to negative reference voltage.
- During reference voltage integration, o/p of integrator is logic 1 between time interval t1 and t2, hence counter will count the pulses for the second time.
- When t > t2 , comparator output is logic 0 and counter will stop.

here $T_1 = 2^N T_C$

T_C = Time period of Clock Pulse

At time T_2 the o/p of voltage of integrator is

$$V_o = -\frac{V_a}{RC} T_1 + \frac{V_R}{RC}(t - T_1)$$

$$0 = -\frac{V_a}{RC} \cdot T_1 + \frac{V_R}{RC}(T_2 - T_1)$$

$$\frac{V_R}{RC}(T_2 - T_1) = \frac{V_a}{RC} T_1$$

$$T_2 - T_1 = \frac{V_a}{V_R} \cdot 2^N T_C \quad \text{—①}$$

let the Count in Counter is n at T_2

$$T_2 - T_1 = n T_C \quad \text{—②}$$

from ① & ②

$$\frac{V_a}{V_R} 2^N T_C = n T_C$$

$$n = \frac{V_a}{V_R} 2^N$$

Gateway Classes

Switched-Capacitor Circuit?

A switched-capacitor circuit is a discrete-time circuit that exploits the charge transfer in and out of a capacitor as controlled by switches.

→ It is used in implementation of filter.

→ It work by moving charge into and out of Capacitor by opening and closing Switches.

→ Also Known as Switch Capaciter Resister.

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With S_1 close $\rightarrow V_i$ applied

S_2 close $\rightarrow V_0$ applied

Net Charge across Capacitor

$$q = CV$$

Now S_1 = close, S_2 = open

$$q_{input} = CV_{in}$$

when S_2 = close, S_1 = open

$$q_{out} = C V_{out}$$

Charge out of Capacitor to o/p is

$$q = q_{in} - q_{out} = C(V_{in} - V_{out})$$

Current is given by

$$I = \frac{dq}{dt} = q \cdot f$$

$$I = q \cdot f = C_s(V_{in} - V_{out}) f$$

Now Let Voltage across Capacitor

$$V = V_{in} - V_{out}$$

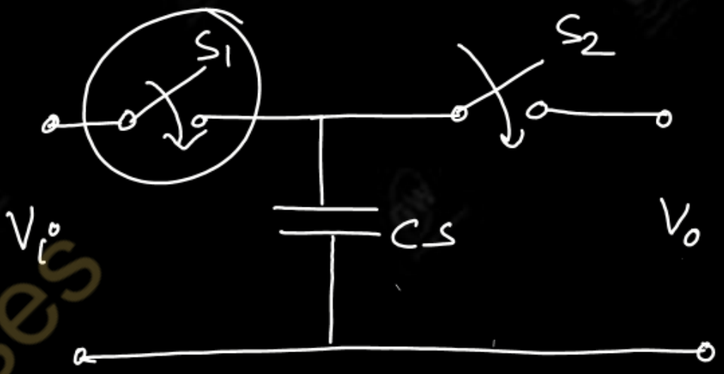
Thus

$$I = C_s V f$$

or

$$\frac{V}{I} = \frac{1}{C_s \cdot f}$$

$$R = \frac{1}{C_s f}$$



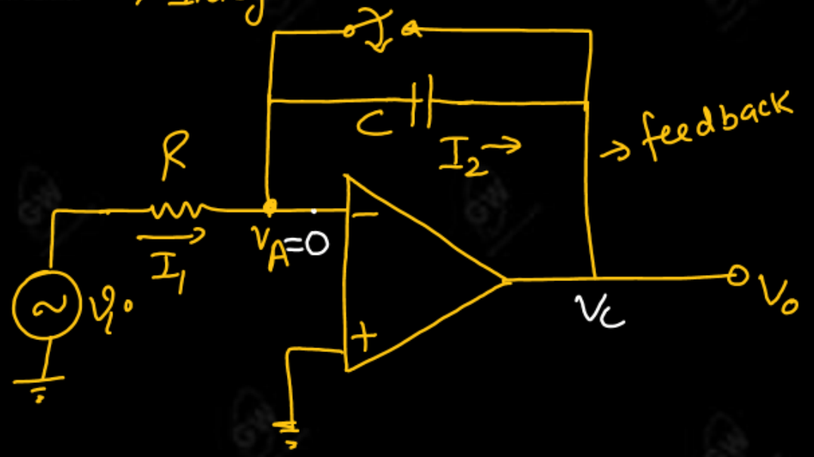
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Application of Switched Capacitor Resistor (

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→ Integrator



Virtually Ground terminal of op-amp so that $V_A = 0$

$$I_1 = I_2$$

$$\frac{V_i - V_A}{R} = C\frac{d(V_A - V_c)}{dt}$$

$$\frac{V_i}{R} = -C\frac{dV_c}{dt}$$

$$\frac{dV_c}{dt} = -\frac{V_i}{RC}$$

$$V_c = -\frac{1}{RC}\int_0^t V_i\,dt$$

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