AKTU

B.Tech III-Sem

Digital System Design

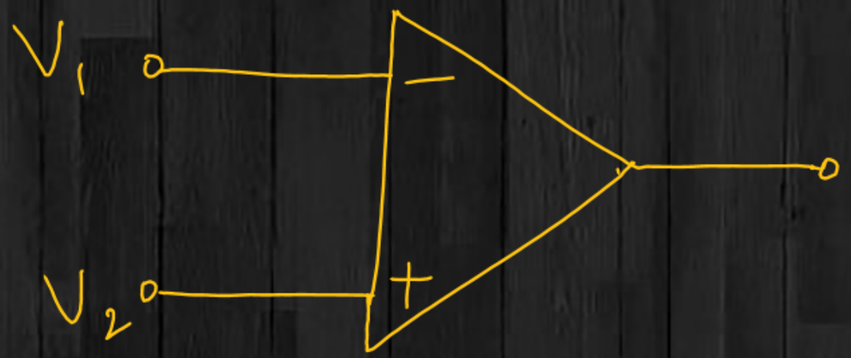


Unit-5 Lecture-3

EC & EC Allied

GATEWAY CLASSES

Gateway classes



$V_1 > V_2 \Rightarrow 0$

$V_2 > V_1 \Rightarrow 1$







Gateway classes

UNIT 5 : Digital-to-Analog converters (DAC)

Lec 3

Today's Target

- Dual Slope type ADC
- **Successive-approximation ADC**
- University Questions

Gateway classes

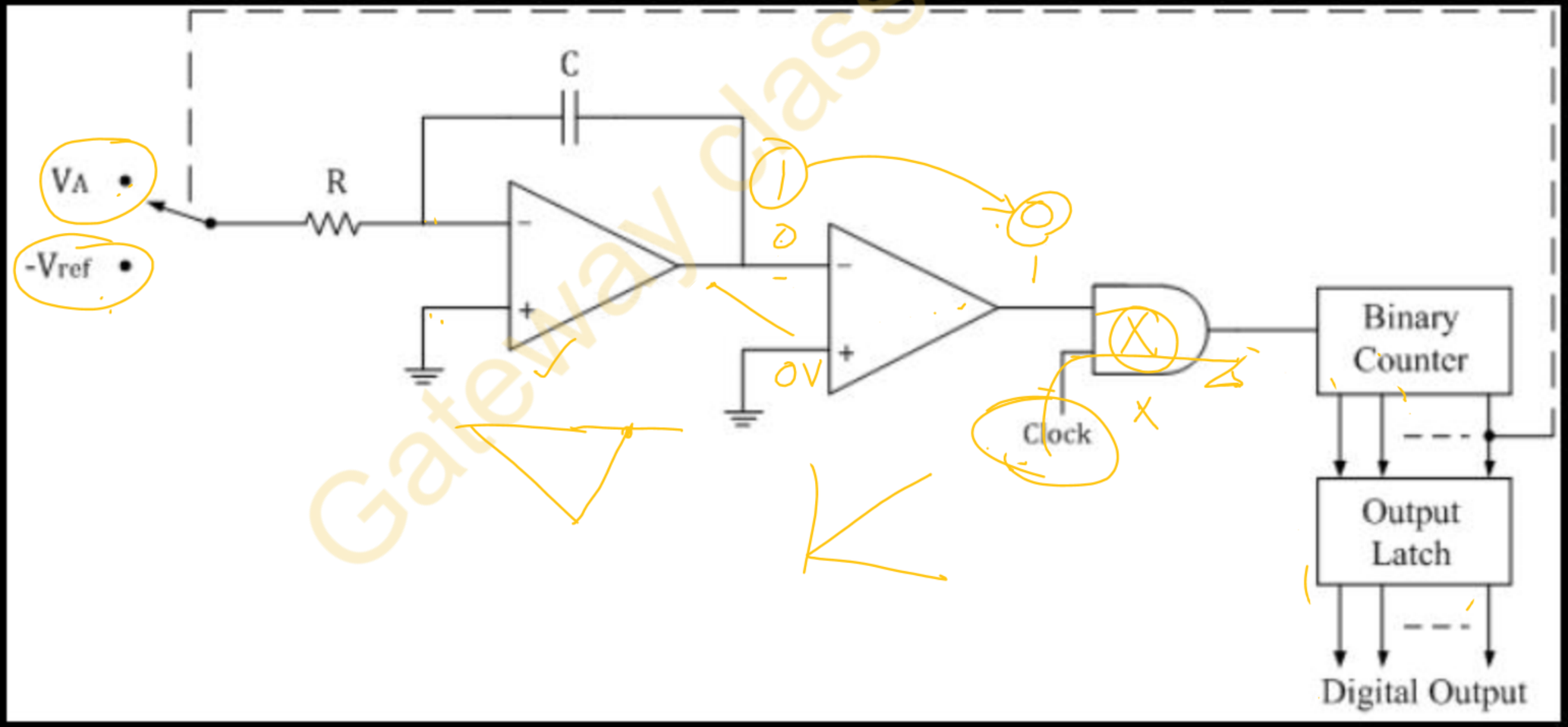
UNIVERSITY QUESTIONS

YEAR	QUESTIONS	MARKS
22-23	Draw and explain the dual slope analog to digital convertor	10 Marks
21-22	Explain single slope and dual slope ADC with a neat sketch.	10 Marks
21-22	List some advantages of successive approximation?	2 Marks
21-22	Where is SAR ADC used?	2 Marks
20-21 19-20	Explain the operation of successive approximation ADC. Discuss it merits and demerits.	10 Marks

Gateway Classes

Dual Slope type ADC

- In dual slope type ADC, the integrator generates two different ramps, one with the known analog input voltage VA and another with a known reference voltage –Vref. Hence it is called as dual slope A to D converter.
- The logic diagram for the same is shown below.



Gateway classes

Operation

- The binary counter & output of integrator is initially reset to 0000 i.e. 0V
- The input to the ramp generator or integrator is switched to the unknown analog input voltage V_A which generates a negative ramp output.
- The output of comparator is positive and the clock is passed through the AND gate resulting in counting up of the binary counter.
- The negative ramp continues for a fixed time period t_1, determined by a count detector and generates ramp output given by; $V_S = - V_A/RC \times t_1$
- When the counter reaches the fixed count at time period t_1, the binary counter resets to 0000 and switches the integrator input to a negative reference voltage –Vref.
- Now the ramp generator starts with the initial value –Vs and increases in positive direction until it reaches 0V and the counter gets advanced.
- When Vs reaches 0V, comparator output becomes negative (i.e. logic 0) and the AND gate is deactivated. Hence no further clock is applied through AND gate.
- Now, the conversion cycle is said to be completed and the positive ramp voltage is given by; $V_S = Vref/RC \times t_2$
- Where Vref & RC are constants and time period t_2 is variable.

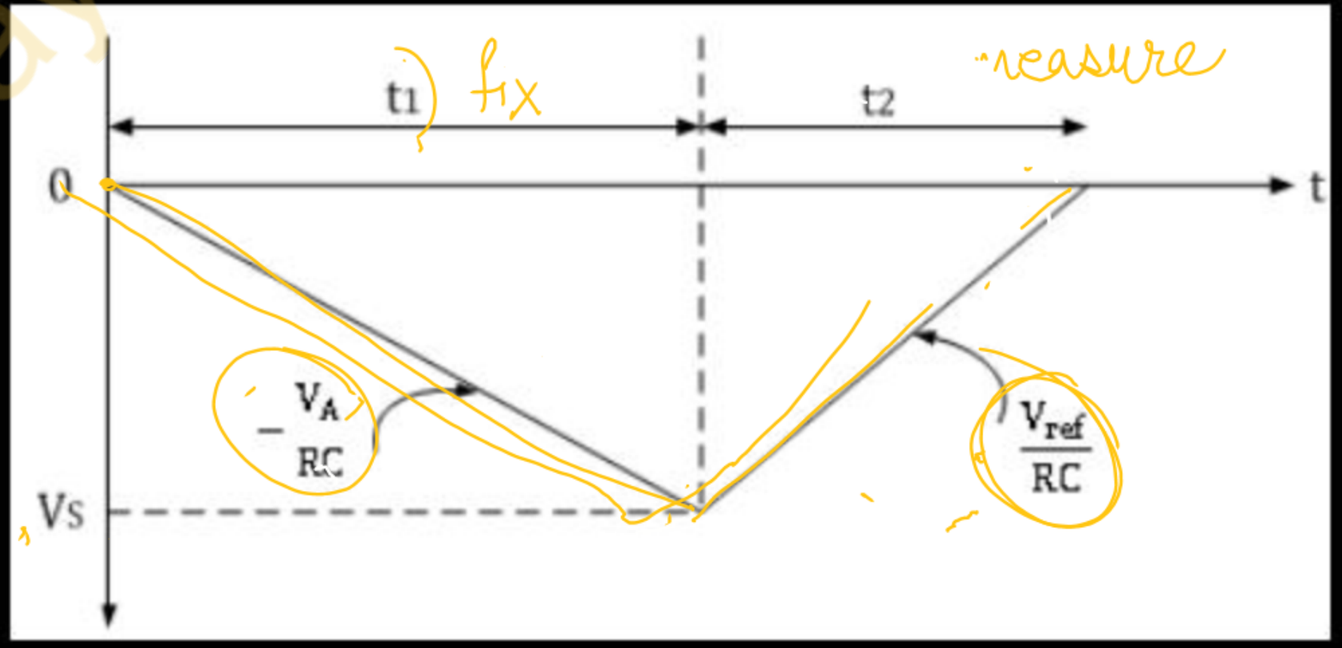
Gateway Classes

The dual ramp output waveform

- Since ramp generator voltage starts at 0V, decreasing down to –Vs and then increasing up to 0V, the amplitude of negative and positive ramp voltages can be equated as follows.
  $\therefore Vref/RC \times t_2 = -VA/RC \times t_1$
  $\therefore t_2 = -t_1 \times V_A / Vref$
  $\therefore V_A = - Vref \times t_2 / t_1$

$V_A \propto t_2$

- Thus the unknown analog input voltage V_A is proportional to the time period t_2, because Vref is a known reference voltage and t_1 is the predetermined time period.
- The binary counter gives corresponding digital value for time period t_2.
- Thus the counter counts digital output as
  Digital output=(counts/sec) t_2
  ∴ Digital output= (counts/sec) $[t_1 \times V_A / Vref]$



Gateway classes

$$-\frac{V_A}{RC} \times t_1 = \frac{V_{ref}}{RC} \times t_2$$

$$V_A = -V_{ref} \times \frac{t_2}{t_1}$$

Gateway Classes

For example

- Consider;
- the clock frequency is 1 MHz,
- the reference voltage is -1V,
- the fixed time period t1 is 1ms and
- the RC time constant is also 1 ms.
- Assuming the unknown analog input voltage amplitude as $V_A = 5V$,
- during the fixed time period t1 , the integrator output Vs is;

$$V_S = - V_A /RC \times t_1 = (-5)/1ms \times 1ms = - 5V$$

- During the time period t_2, ramp generator will integrate all the way back to 0V.

$$\therefore t_2 = V_S /Vref \times RC = (-5)/(-1) \times 1ms = 5ms = 5000\mu s$$

- Hence the 4-bit counter value is 5000
- By activating the decimal point of MSD seven segment displays, the display can directly read as 5V.

$$V_S = -\frac{V_A}{RC} \times t_1 = -\frac{5}{1ms} \times 1ms$$

$$V_S = -5$$

$$= -\frac{V_{ref}}{RC} \times t_2 = \frac{-1}{1ms} \times t_2$$

$$-5 = \frac{-1}{1ms} \times t_2$$

$$-5ms = -t_2$$

$$t_2 = 5ms$$

Gateway classes

Successive-approximation ADC

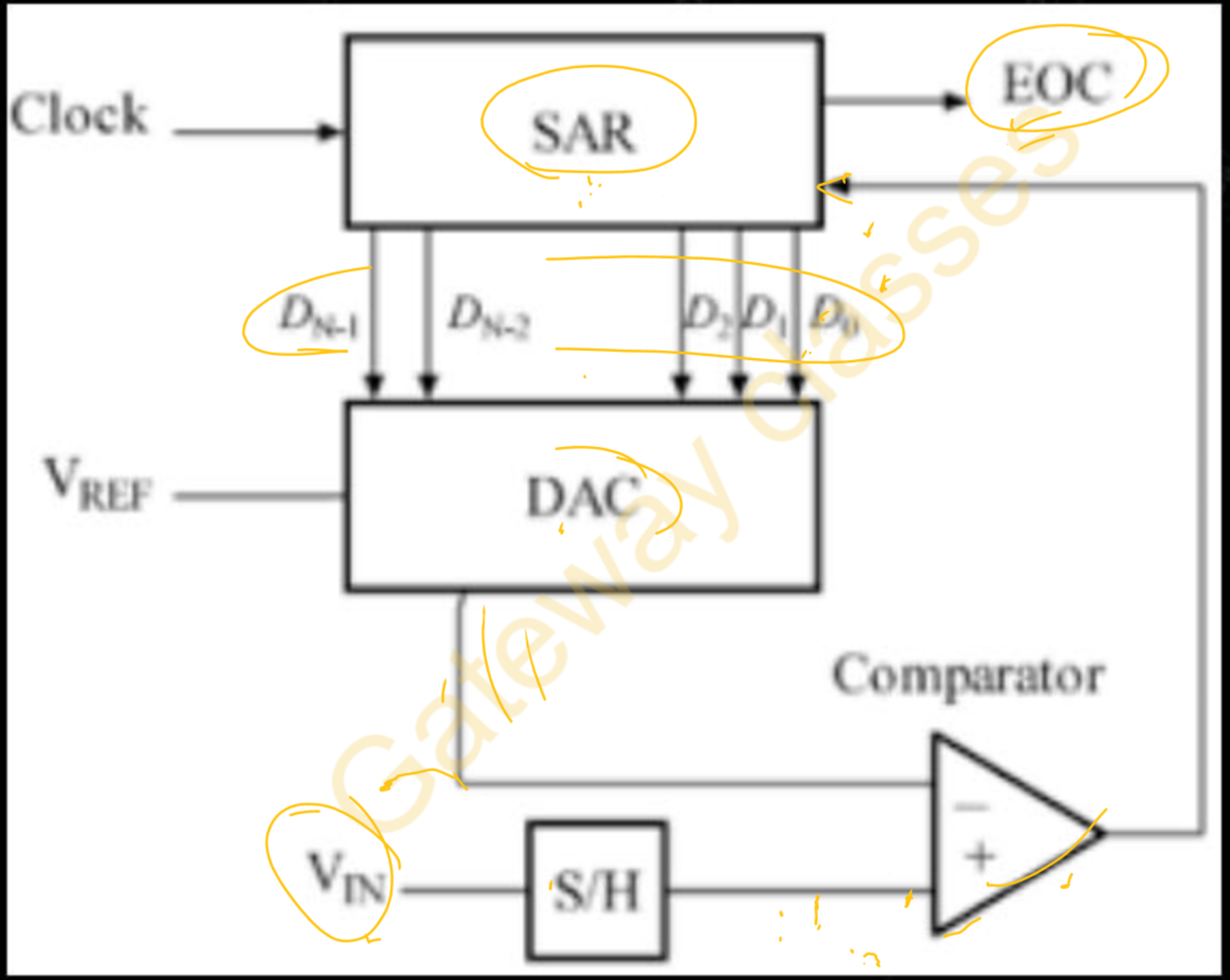
- A successive-approximation ADC is a type of ADC that uses a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.
- The only change in this design is a very special counter circuit known as a successive-approximation register. (SAR)



- This register counts by trying all values of bits starting with the most-significant bit and finishing at the least-significant bit.
- Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly.
- The way the register counts is identical to the "trial-and-fit" method
- The advantage to this counting strategy is much faster results.

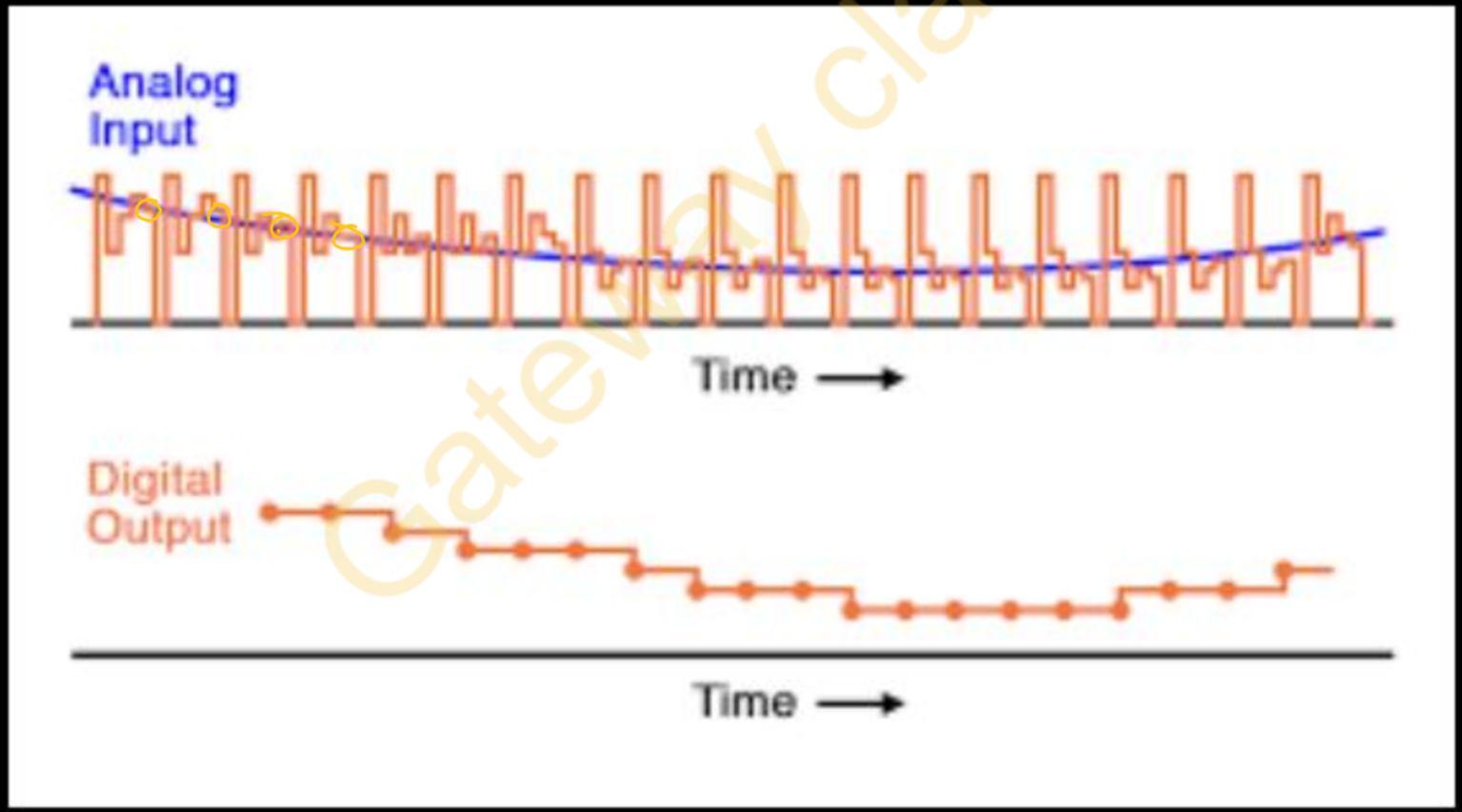
Gateway classes

Successive-approximation ADC



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- SAR is generally capable of outputting the binary number in serial (one bit at a time) format, thus eliminating the need for a shift register.
- Plotted over time, the operation of a successive-approximation ADC looks like this:



Gateway classes

GATEWAY CLASSES

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Thank You