A K T U

B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-4 Lec-3



Today's target

- CMOS Logic families
- PYQ

Avinash Sir

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT- 4

- Logic families and semiconductor memories: TTL NAND gate, specifications, noise margin, propagation delay, fan-in, fan-out, tristate TTL, ECL, CMOS families and their interfacing, memory elements, concept of programmable logic devices like FPGA, logic implementation using programmable devices.

Gateway Classes

MOS Families

Digital circuits with MOSFETs can be grouped into three categories :

- PMOS – uses only P-channel enhancement MOSFETs,
- NMOS - uses only N-channel enhancement MOSFETs, and
- CMOS (complementary MOS) - uses both P and N-channel devices.

Gateway Classes

CMOS Inverter

AKTU 2024-25,23-24,22-23,21-22

It consists of two MOSFETs in series in such a way that the p-channel device has its source connected to + VDD (a positive voltage) and the n-channel device has its source connected to ground. The gates of the two devices are connected together as the common input and the drains are connected together as the common output.

1. When input is HIGH, the gate of Q_2 (p-channel) is at 0 V relative to the source of Q1 i.e. $V_{gS1} = 0$ V. Thus, Q_1 is OFF. On the other hand, the gate of Q_2 (n-channel) is at +VDD relative to its source i.e. V_{gS2} = +VDD. Thus, Q_2 is ON. This will produce $V_{OUT} \sim 0$ V, as shown in the Fig. (a).

2. When input is LOW, the gate of Q_1 (p-channel) is at a negative potential relative to its source while Q2 has Vgs = 0 V. Thus, is ON and Q_2 is OFF. This produces output voltage approximately + VDD, as shown in the Fig. (b).

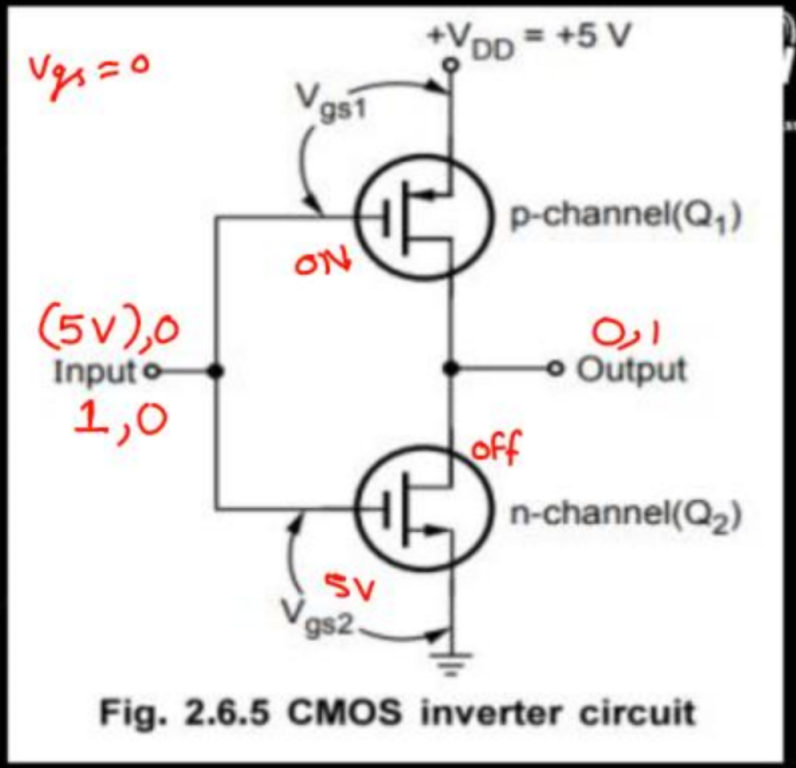
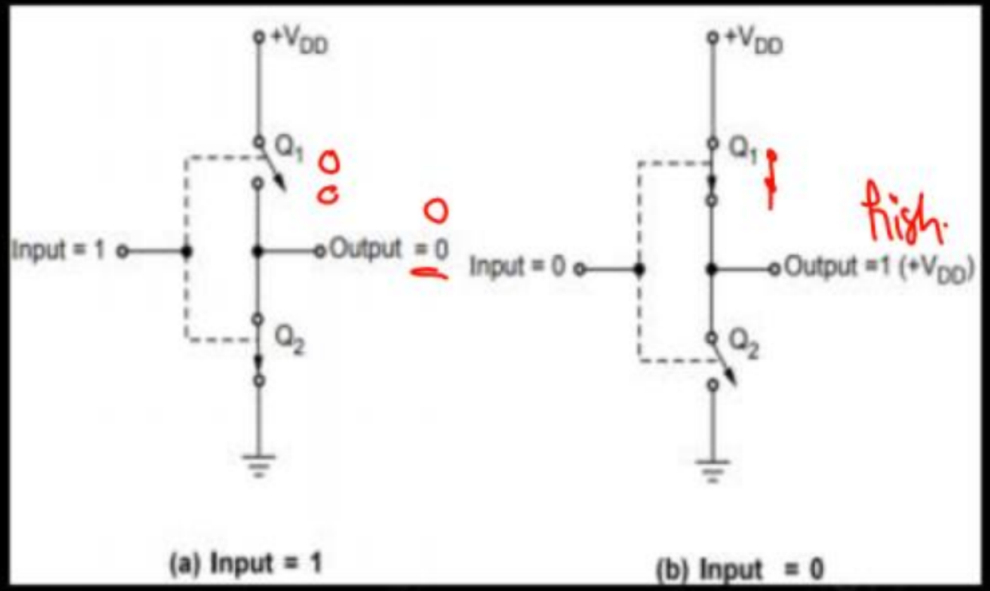


Fig. 2.6.5 CMOS inverter circuit



Gateway Classes

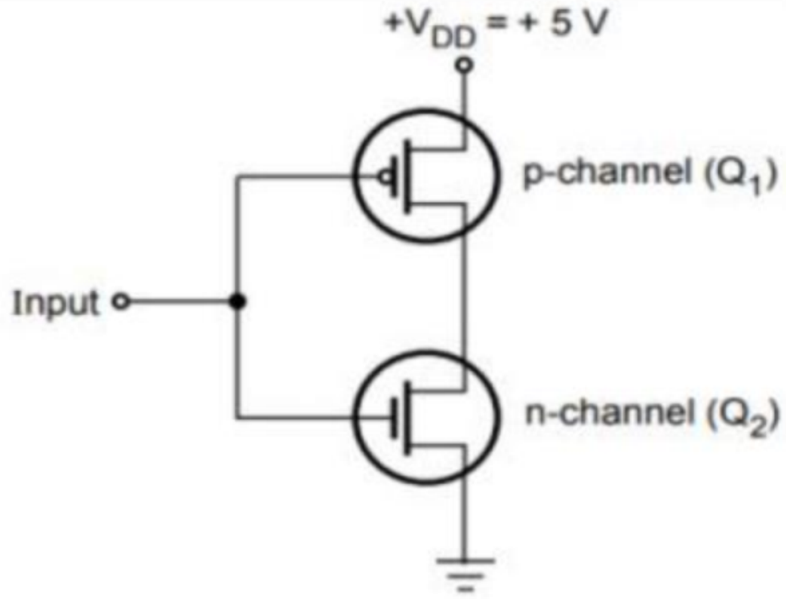
The operation of CMOS inverter circuit.

A	Q_1	Q_2	Output
0	ON	OFF	1
1	OFF	ON	0

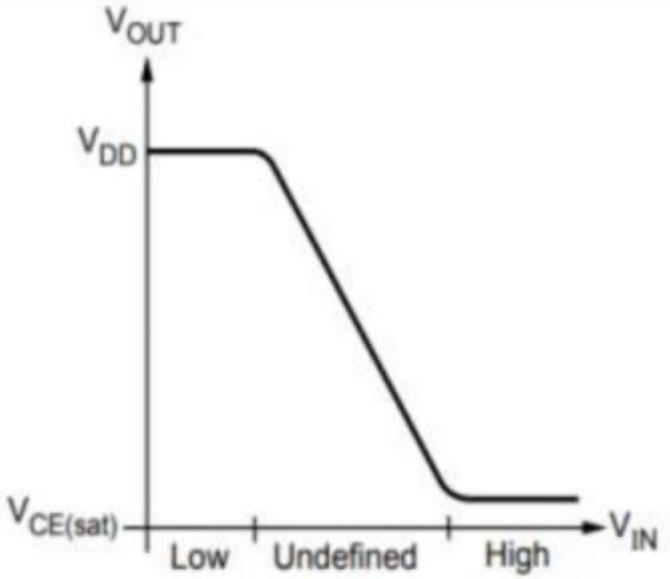
Table 2.6.4 Truth table of inverter

The Fig. shows, different symbols used for the p-channel and n-channel transistors to reflect their logical behaviour. The n-channel transistor (Q2) is switched 'ON' when a HIGH voltage is applied at the input. The p-channel transistor (Qi) has the opposite behaviour, it is switched ON when a LOW voltage is applied at the input. It is indicated by placing bubble in the symbol.

The Fig. shows the transfer characteristics of CMOS inverter.



The CMOS inverter

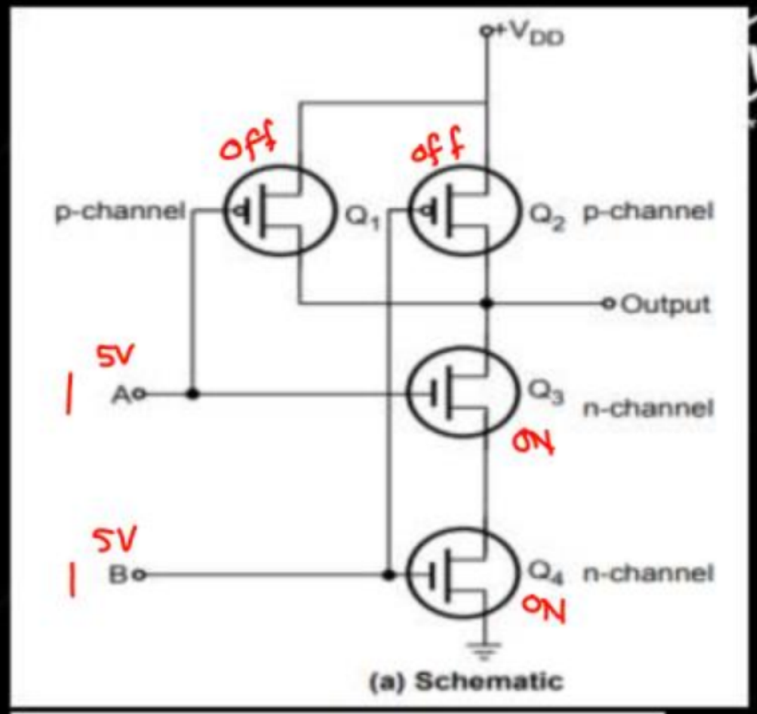


CMOS inverter transfer characteristics

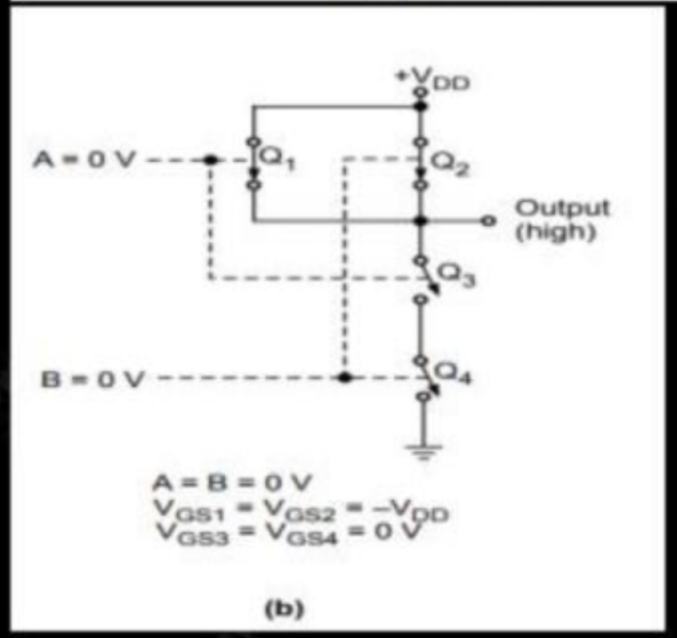
Gateway Classes

COMS NAND Gate

- Fig. shows CMOS 2-input NAND gate. It consists of two p-channel MOSFETs, Q4 and Q2, connected in parallel and two n-channel MOSFETs, Q3 and Q4 connected in series.
- Fig.(a) shows the equivalent switching circuit when both inputs are low. Here, the gates of both p-channel MOSFETs are negative with respect to their sources, since the sources are connected to + VDD.
- Thus, Q1 and Q2 are both ON. Since the gate-to-source voltages of Q3 and Q4 (n-channel MOSFETs) are both 0 V, those MOSFETs are OFF.
- The output is therefore connected to +VDD (HIGH) through Q4 and Q2 and is disconnected from ground, as shown in the Fig. (b)



(a) Schematic

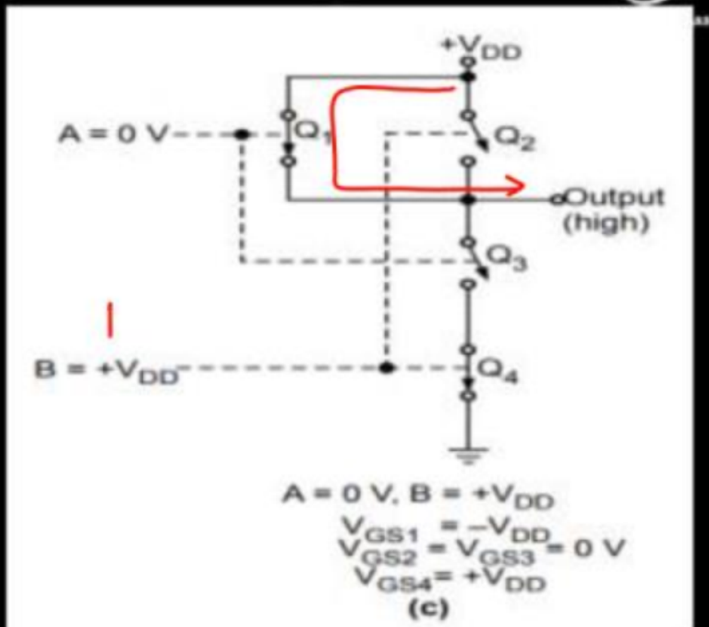


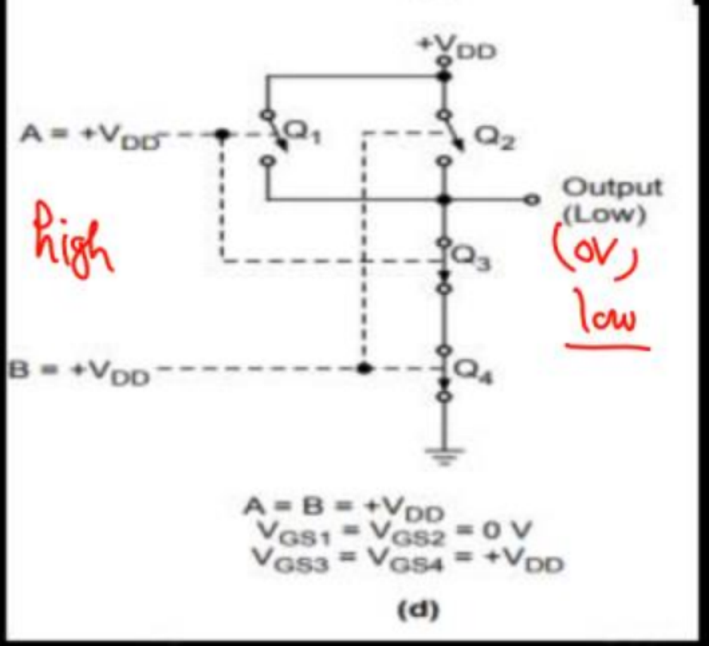
(b)

Gateway Classes

COMS NAND Gate

- Fig. (c) shows the equivalent switching circuit when A = 0 and B = +VDD. In this case, Q4 is on because VGSi= - VDD and Q4 is ON because VGg4 = +VDD.
- MOSFETs Q2 and Q3 are off because their gate-to-source voltages are 0 V. Since Q4 is ON and Q3 is OFF, the output is connected to +VDD and it is disconnected from ground.
- When A = +VDD and B = 0 V, the situation is similar (not shown); the output is connected to +VDD through Q2 and it is disconnected from ground because Q4 is OFF.
- Finally, when both inputs are high (A = B = +VDD), MOSFETs Q1 and Q2 are both OFF and Q3 and Q4 are both ON. Thus, the output is connected to the ground through Q3 and Q4 and it is disconnected from + VDD.





Gateway Classes

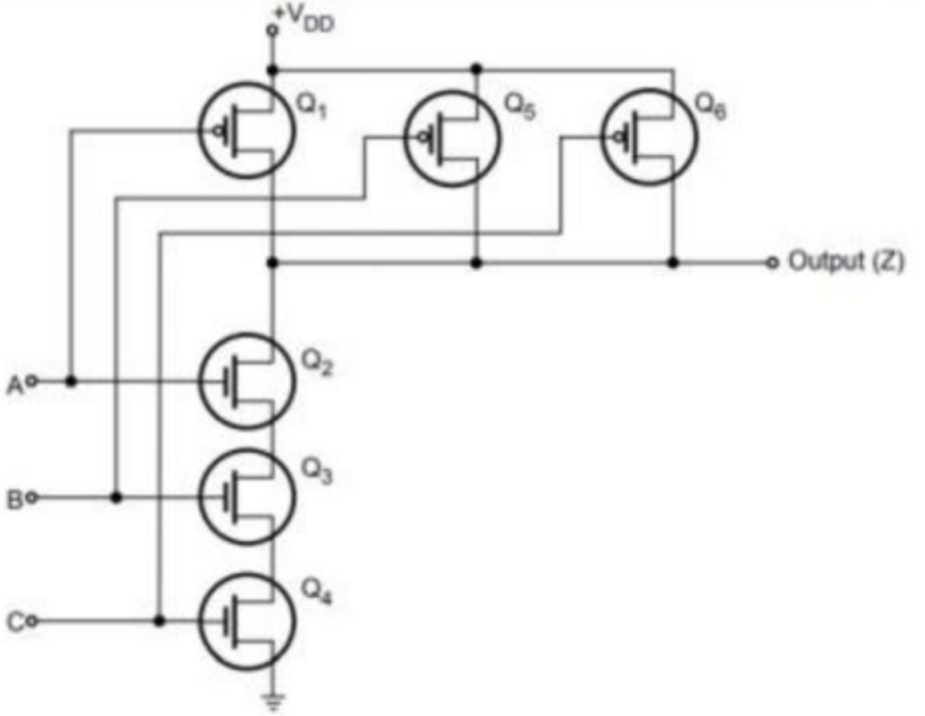
COMS NAND Gate

- The Table summarizes the operation of 2-input CMOS NAND gate.

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Table 2.6.5 Truth table of NAND gate

- Note : p-channel MOSFET is ON when its gate voltage is negative with respect to its source whereas n-channel MOSFET is ON when its gate voltage is positive with respect to its source
- The Fig. shows the circuit diagram, function table and logic symbol of CMOS 3-input NAND gate.



(a) Circuit diagram

A	B	C	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0	0	ON	OFF	OFF	OFF	ON	ON	1
0	0	1	ON	OFF	OFF	ON	ON	OFF	1
0	1	0	ON	OFF	ON	OFF	OFF	ON	1
0	1	1	ON	OFF	ON	ON	OFF	OFF	1
1	0	0	OFF	ON	OFF	OFF	ON	ON	1
1	0	1	OFF	ON	OFF	ON	ON	OFF	1
1	1	0	OFF	ON	ON	OFF	OFF	ON	1
1	1	1	OFF	ON	ON	ON	OFF	OFF	0

(b) Function table

Gateway Classes

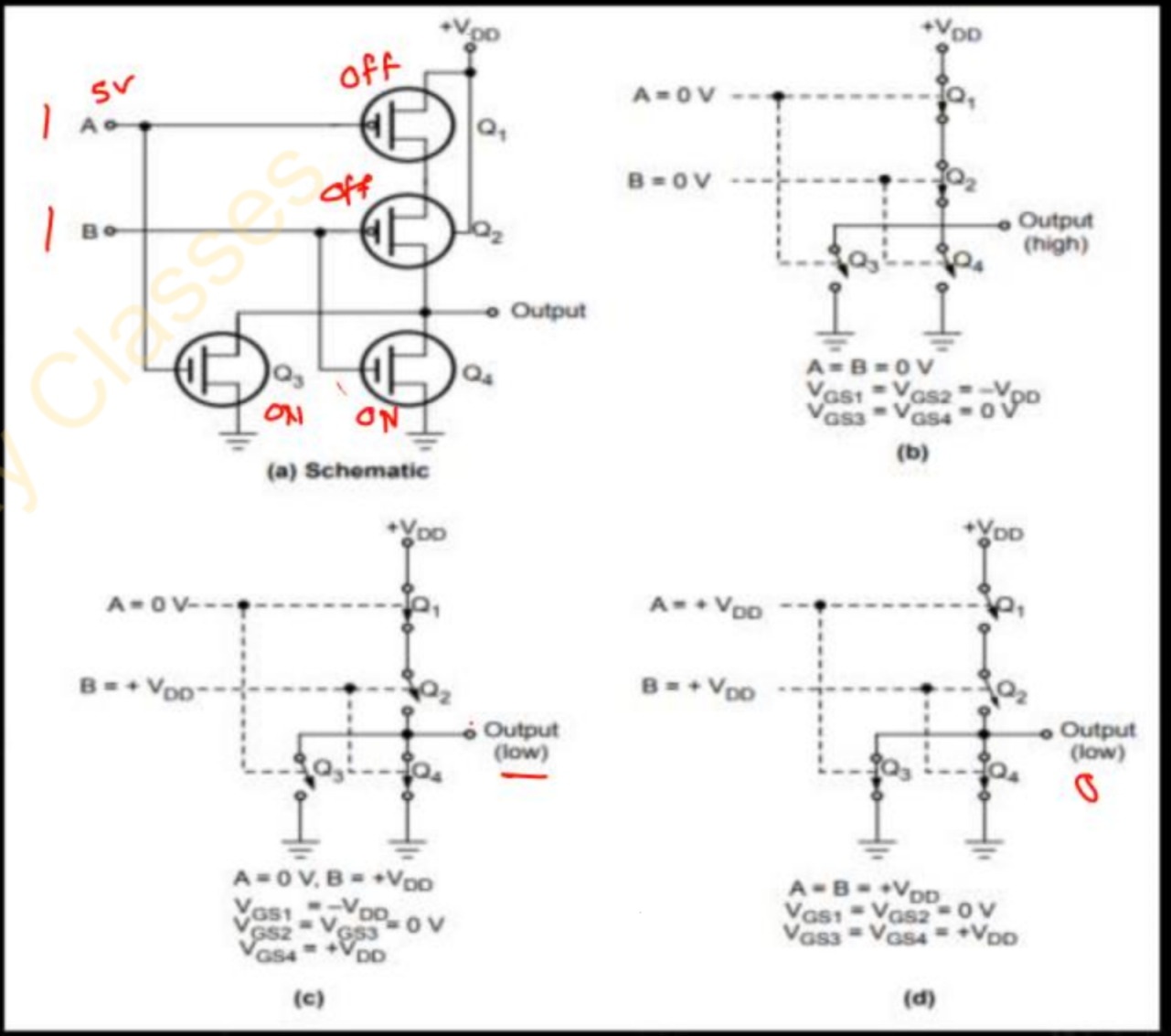
COMS NOR Gate

➢ shows 2-input CMOS NOR gate. Here, p-channel MOSFETs and Q2 are connected in series and n-channel MOSFETs Q3 and Q4 are connected in parallel.

Like NAND circuit, this circuit can be analyzed by realizing that a LOW at any input turns ON its corresponding p-channel MOSFET and turns OFF its corresponding n-channel MOSFET, and vice versa for a HIGH input. This is illustrated in Fig. 2.6.11. The Table 2.6.6 summarizes the operation of 2-input NOR gate.

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Table 2.6.6 Truth table for NOR gate



Gateway Classes

Advantages and Disadvantages of CMOS Family

Advantages

- 1. Consumes less power.
- 2. Can be operated at high voltages, resulting in improved noise immunity.
- 3. Fan-out is more.
- 4. Better noise margin.

Disadvantages

- 1. Susceptible to static charge.
- 2. Switching speed low.
- 3. Greater propagation delay

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