AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design



Unit-4 Lec-1

Today's target

- Logic families
- TTL NAND gate
- Noise margin, propagation delay, fan-in, fan-out, tristate TTL
- PYQ

Avinash Sir

Gateway Classes

AKTU : ***DIGITAL SYSTEM DESIGN (BEC-302)*** **Syllabus**

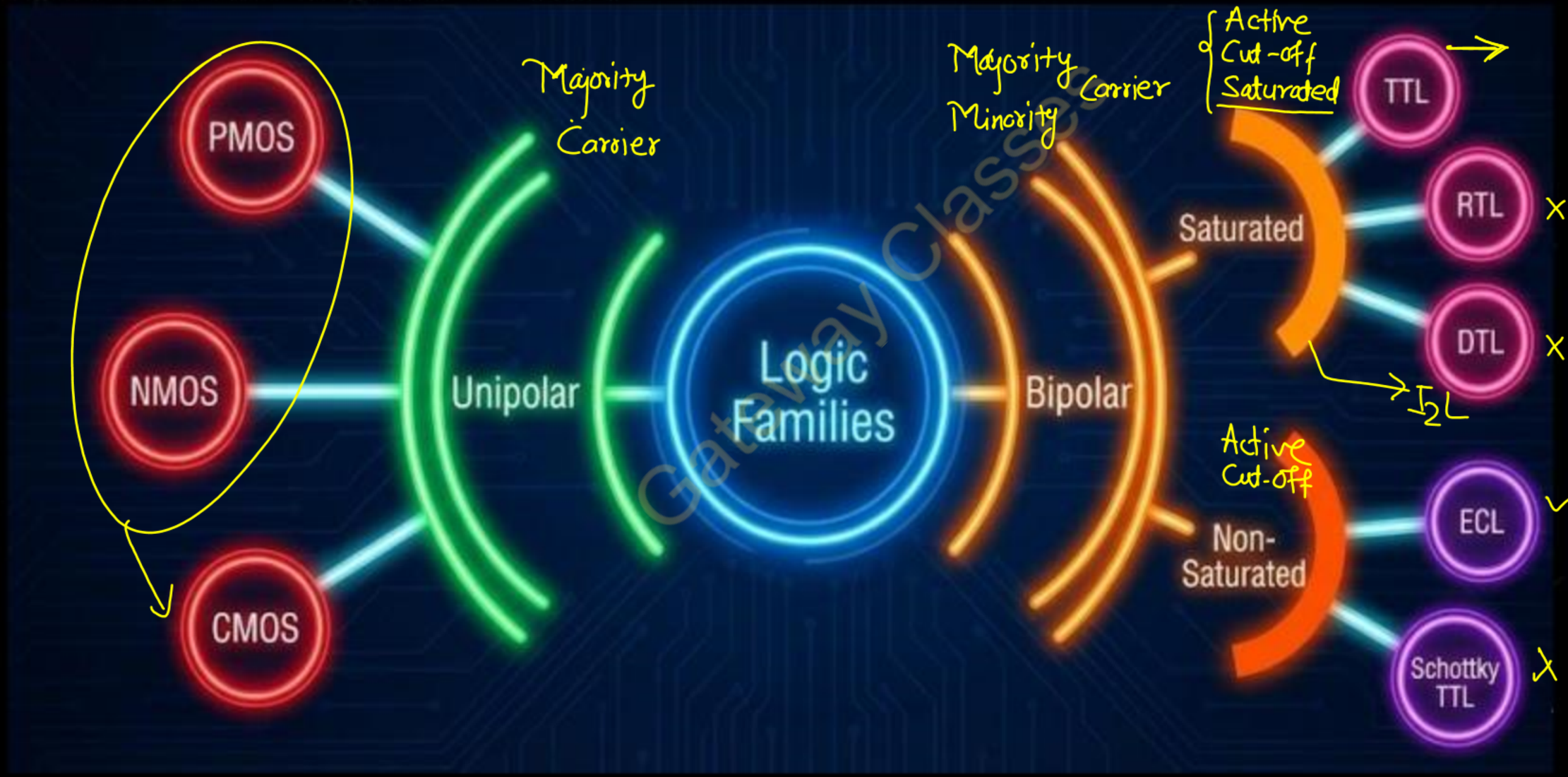
UNIT- 4

- Logic families and semiconductor memories: TTL NAND gate, specifications, noise margin, propagation delay, fan-in, fan-out, tristate TTL, ECL, CMOS families and their interfacing, memory elements, concept of programmable logic devices like FPGA, logic implementation using programmable devices.

Gateway Classes

Logic Families

it is a group of compatible ICs with the same logic levels and supply voltages fabricated for performing various logical functions.



Characteristics of a Logic Family

(speed of operation)

1. Propagation Delay This is the "reaction time" of the logic gate. It measures how fast a signal travels through the gate.

Definition: The time interval between the application of an input signal and the change in the output signal.

Measurement: It is measured in nanoseconds (n_s) or picoseconds (p_s).

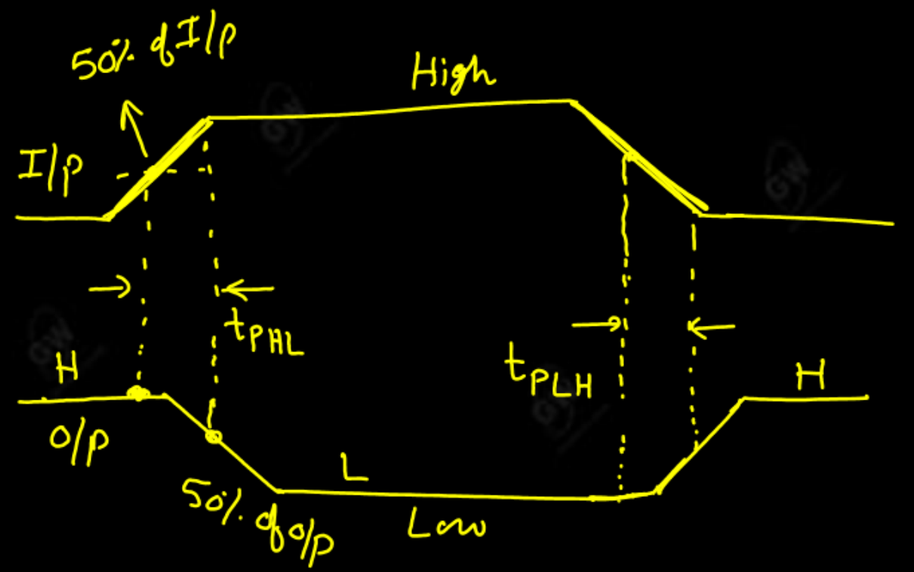
It is usually defined by two specific metrics:

t_{PHL} : Time taken for the output to switch from High to Low.

t_{PLH} : Time taken for the output to switch from Low to High.

Average Delay: $t_{pd} = (t_{PHL} + t_{PLH})/2$

Significance: This limits the maximum speed (frequency) at which a digital system can run. If the delay is too long, the next stage of the circuit won't receive the data in time.



Gateway Classes

Transistor-Transistor Logic (TTL) as NAND Gate Operation

Logic levels in TTL:

Logic 0 ≈ VCE(sat) ≈ 0.2 V

Logic 1 ≈ VCC = 5 V

For p–n junction (diode operation)

Voltage across a conducting diode ≈ 0.7 V

Cut-in (threshold) voltage ≈ 0.6 V

For Transistor

Base–Emitter voltage in saturation (V_{BE},sat) ≈ 0.8 V

Base–Emitter cut-in voltage (V_{BE}cut-in) ≈ 0.5 V

Collector–Emitter saturation voltage (V_{CE},sat) ≈ 0.2 V

Gateway Classes

Power dissipation :-

⇒ Power supply by V_{cc} . dissipate in form of heat

Power dissipation = $V_{cc} . I_{cc}$

Power dissipation is generally in milli watt.

Figure of merit :

= Power dissipation × Propagation delay.

Ex. F.O.M = 5mW × 2ns

= 10 P. Joule.

Gateway Classes

Characteristics of a Logic Family

2. Noise Margin (Immunity):- In the real world, signals are never perfect. "Noise" (unwanted electrical interference) often gets added to the signal as it travels through wires. The Noise Margin is the safety buffer that ensures a logic gate doesn't mistake a "High" signal for a "Low" one (or vice versa) due to this noise.

Definition: The maximum noise voltage that can be added to an input signal without causing an error in the output. Logic gates have a "legal" range for High and Low voltages.

V_{OH}: Minimum voltage a gate outputs for a HIGH.

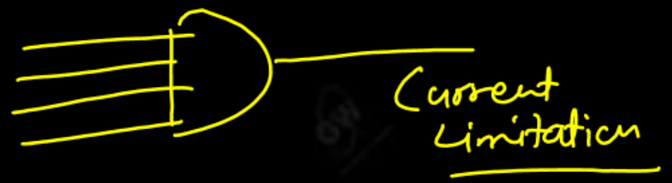
V_{IH}: Minimum voltage a gate accepts as a HIGH.

The difference V_{OH} - V_{IH} is the High-State Noise Margin (NM_H).

Similarly, the Low-State Noise Margin (NM_L) is the difference between what a gate accepts as Low (V_{IL}) and what the previous gate outputs as Low (V_{OL}).

Gateway Classes

Characteristics of a Logic Family



3. Fan-in : This is a physical limitation of the input side of the gate. The number of inputs that a single logic gate is designed to handle.

Example: A 2-input NAND gate has a fan-in of 2; an 8-input NAND gate has a fan-in of 8.

4. Fan-out This is the "muscle" or driving capability of the gate's output. The maximum number of standard inputs (loads) of the same logic family that a single logic gate output can drive reliably.

Current Limit (DC Fan-out): In families like TTL, the output transistor must sink or source current for every input it drives. If you connect too many inputs, the output voltage will drop (or rise) into the "forbidden" zone, causing errors.

Speed Limit (AC Fan-out): In families like CMOS, the inputs are capacitors. Adding more inputs adds more "capacitive load." The gate might still work, but it will take much longer to charge up all those capacitors, drastically increasing Propagation Delay.

Gateway Classes

Transistor-Transistor Logic (TTL)

The Transistor-Transistor Logic (TTL) is a logic family made up of BJTs (bipolar junction transistors. The best examples of TTL are logic gates namely the 7402 NOR Gate & the 7400 NAND gate.

It is a digital logic family that uses bipolar junction transistors (BJTs) for both Input switching & Output driving. Supply voltage is +5V DC.

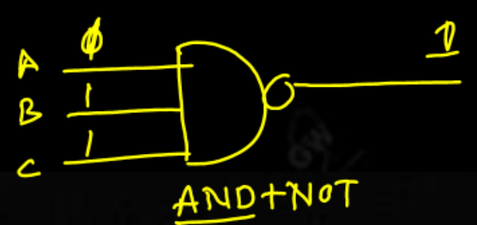
In DTL, diodes are used in the input stage, which cause large delay due to diode storage time. TTL uses transistors instead of diodes, resulting in much faster switching.

It also offers Higher Noise Immunity, Better Fan-out Capability, Improved Temperature Stability

Gateway Classes

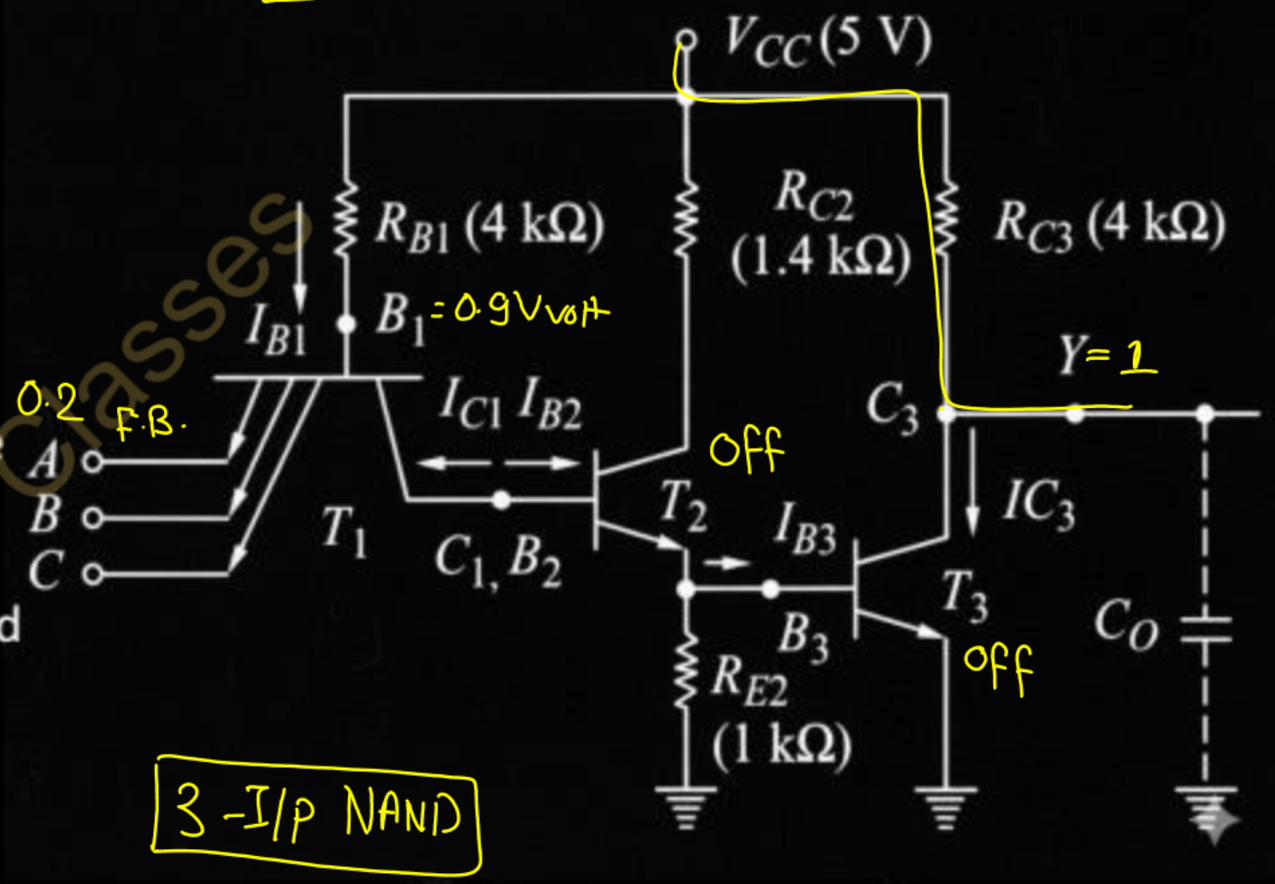
Transistor-Transistor Logic (TTL) as NAND Gate

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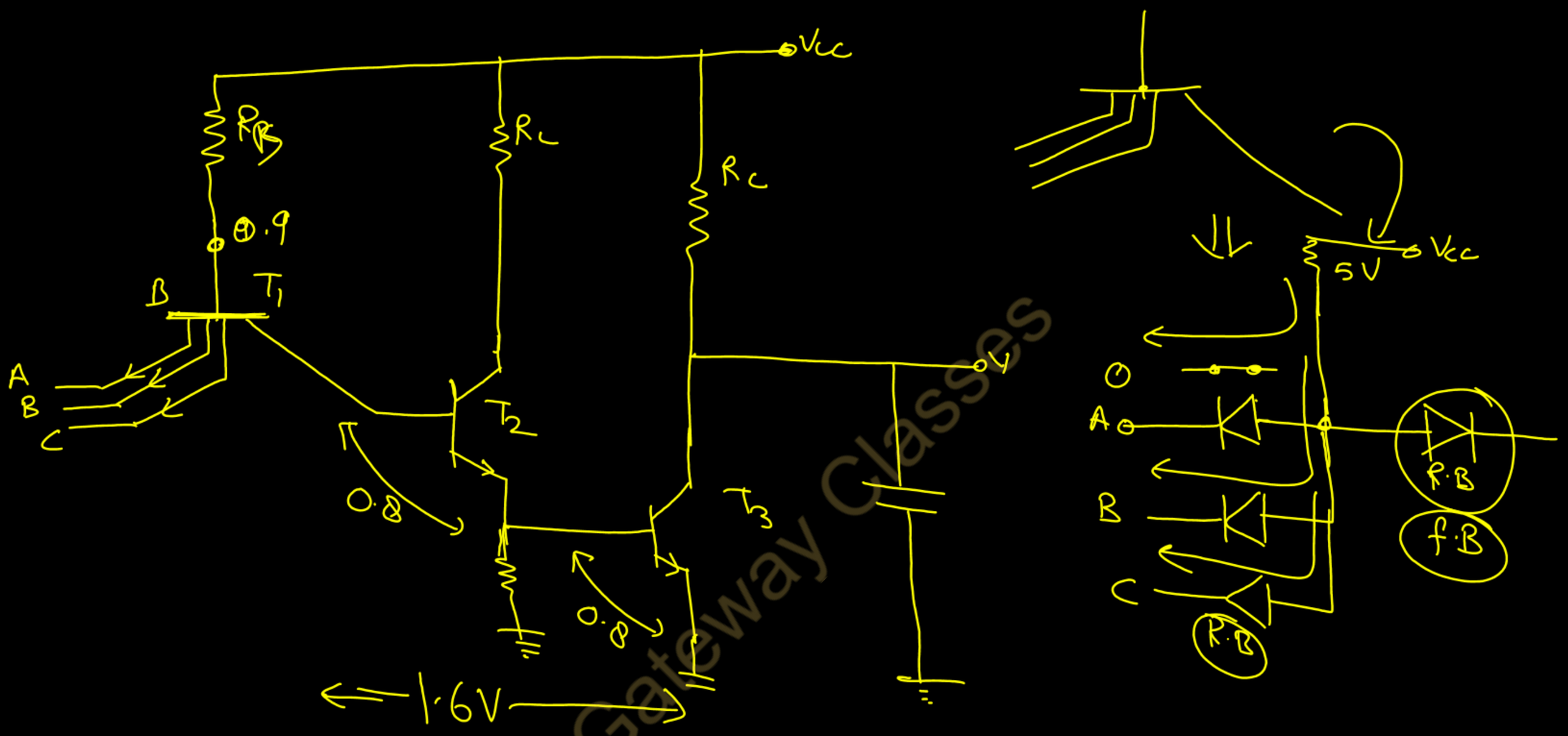


Operation :- For NAND Gate output is low when all inputs are high if any input is low output is always high.

- **Case-1 (When at least one input is low)**
- The emitter-base junction of transistor T1 becomes forward biased.
- T1 enters into forward active mode, establishing a base voltage of VB1 = 0.9V.
- For the base-collector junction of T1 to become forward biased—and for transistors T2 and T3 to conduct—the voltage VB1 is required to be at least 1.6V.
- Since the actual voltage is insufficient (0.9V is less than the required 1.6V), transistors T2 and T3 remain in cut-off. And the output (o/p) will be high.



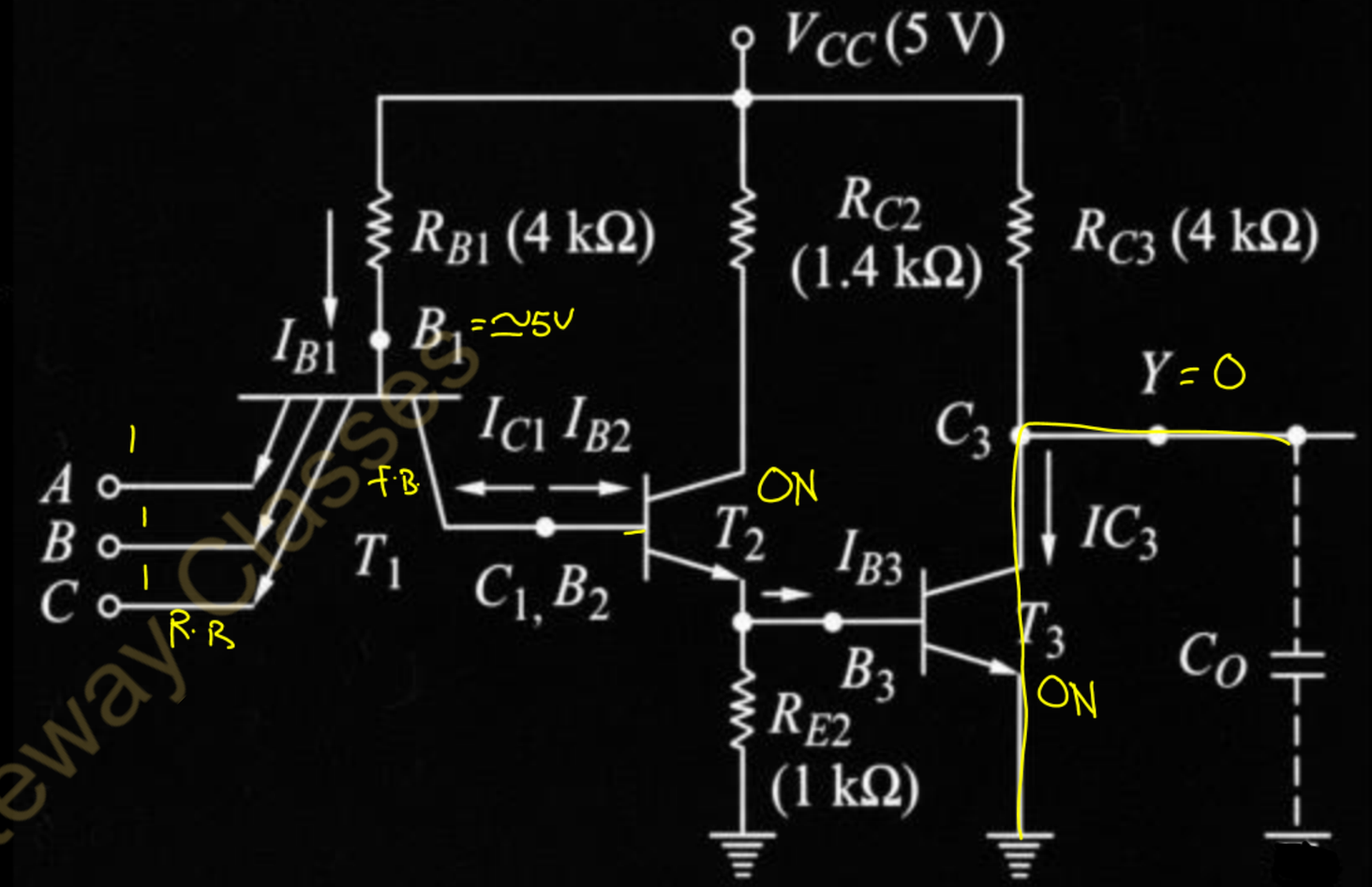
Gateway Classes



Gateway Classes

Case-2 (When all inputs are high)

- The emitter-base junction of transistor T1 becomes reversed biased.
- Point is connected to Vcc.
- Base current is supplied to drive the T2 & T3.
- T2 & T3 goes into saturation (ON)
- So out put will be equal to 0.2 volt (Low)
- So the NAND Gate Operation is verified.



Gateway Classes

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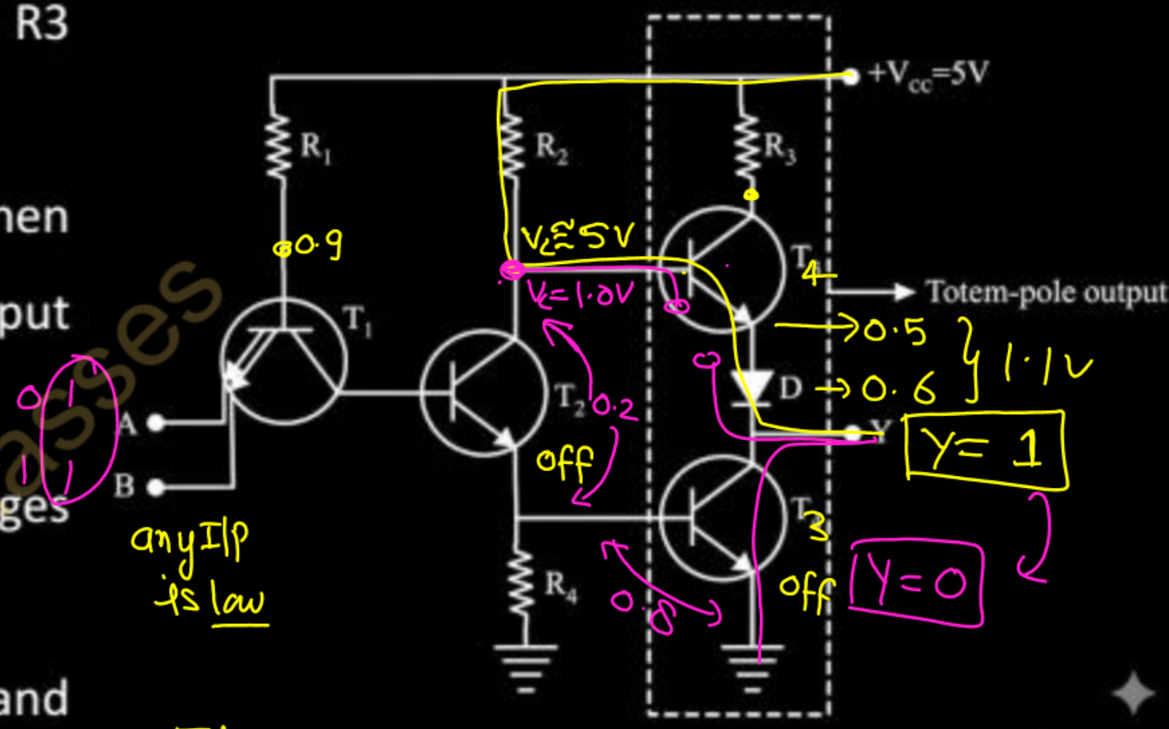
Output configuration of TTL

1. Totem-pole output
2. open collector output
3. Tri-state gate output

Gateway Classes

Totem-pole output

- Transistor T3, T4, diode D and current limiting resistor R3 form the totem-pole output configuration of TTL.
- There are a few advantages of using this configuration. When the output switches from LOW to a HIGH state, the output transistor T4 goes from saturation to cut off.
- During this transition, the load capacitance across T3 charges exponentially from low to a high voltage level.
- Due to the low output impedance of both transistors T3 and T4, the output voltage can change quickly from LOW to HIGH value as the capacitance charge and discharge quickly.



(i) If Any I/p is low
T_2 & T_3 = off, $V_c = V_{cc}$, T_4 & D Conduct, Y=1

(ii) If both I/p is high
T_2 & T_3 = ON, $V_c = 0.2 + 0.8 = 1V$, It is insufficient to conduct T_4 & D. Hence o/p Y is connected to ground Y=0

Gateway Classes

Totem-Pole Output Advantages

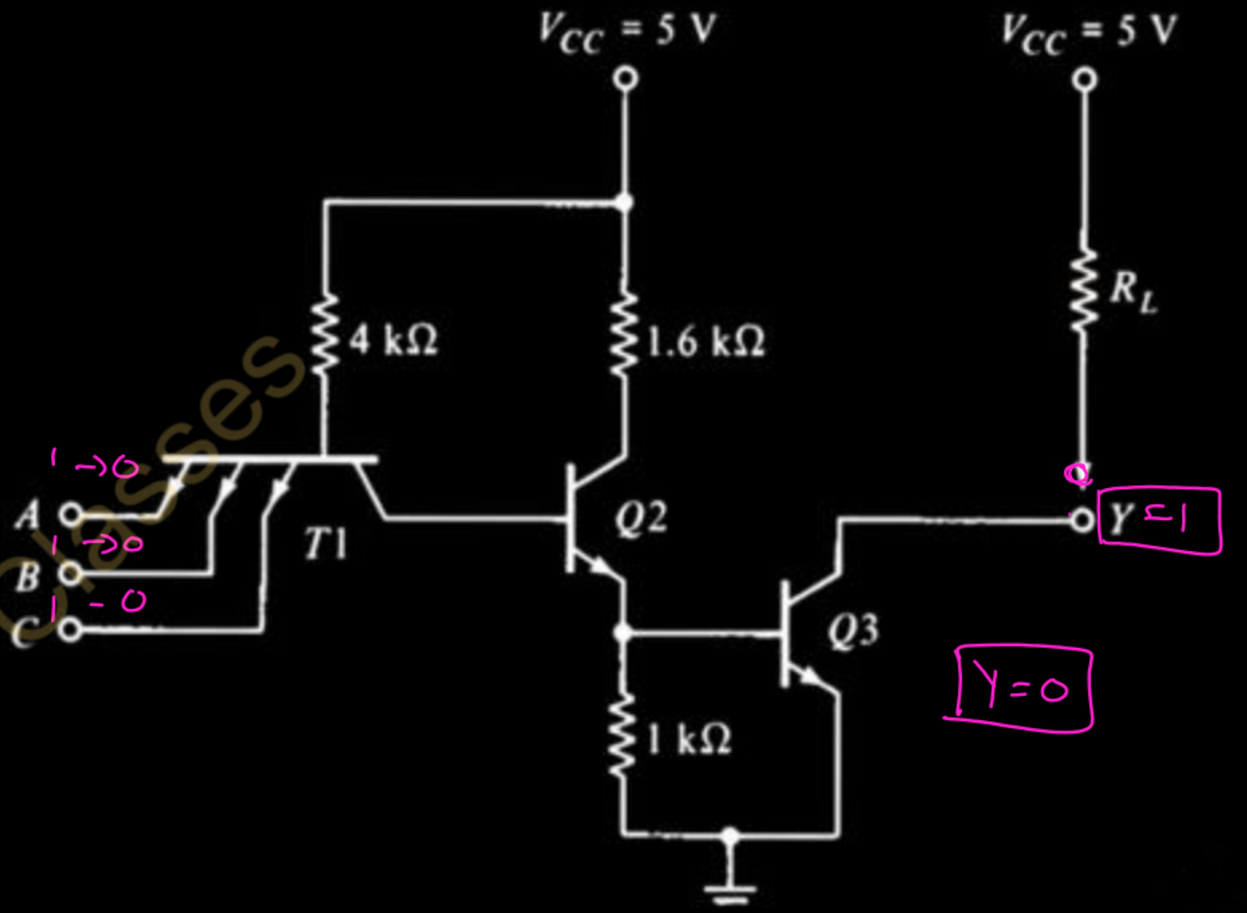
- ***High speed switching*** → Due to push-pull action (one transistor sources current while the other sinks), output changes state quickly.
- ***Low output impedance*** → Provides strong drive current to the next stage; minimizes propagation delay.
- ***Well-defined output voltage levels*** → Logic HIGH is close to Vcc and logic LOW close to ground.
- ***Less power dissipation at static states*** → Current flows only during switching moments.
- **Limitations**
- ***Cannot be wired-OR / wired-AND*** → Outputs must not be directly connected together; doing so may cause short-circuit between HIGH and LOW drivers.
- ***Noise spikes during switching*** → Due to cross-conduction (both transistors may momentarily conduct).
- ***Requires precise timing design*** → Shoot-through current must be controlled to avoid heating and damage.
- ***Not suitable for driving large loads*** → Limited current for external devices like relays, motors, lamps.

Gateway Classes

Open collector output

With any of the input at logic low, the corresponding emitter-base junction is forward biased and the voltage drop across the base of T1 is around 0.9V, not enough for the transistors T2 and T3 to conduct. Thus the output is either floating or Vcc, i.e. High level.

Similarly, when all inputs are high, all base-emitter junctions of T1 are reverse biased and transistor T2 and T3 get enough base current and are in saturation mode. The output is at logic low.



Gateway Classes

Open collector output

Advantages

- ***Supports wired-OR / wired-AND logic*** → Multiple outputs can be tied together using a pull-up resistor.
- ***Can interface with different voltage levels*** , Example: TTL 5V output can drive 12V logic using pull-up.
- ***Ideal for driving high-power loads*** → Relays, motors, LEDs can be driven using an external power supply.
- ***Easy to use in bus systems and multi-source signaling*** → One line shared by many drivers.

Limitations

- ***Slower switching*** → Rising edge is slow because output goes HIGH through pull-up resistor (passive pull-up).
- ***Higher power consumption*** → Pull-up resistor continuously draws current when output is LOW.
- ***Output HIGH level depends on pull-up value and load*** → Might not be ideal for fast / high-fan-out logic.
- ***Extra components required*** → A pull-up resistor must be added externally.

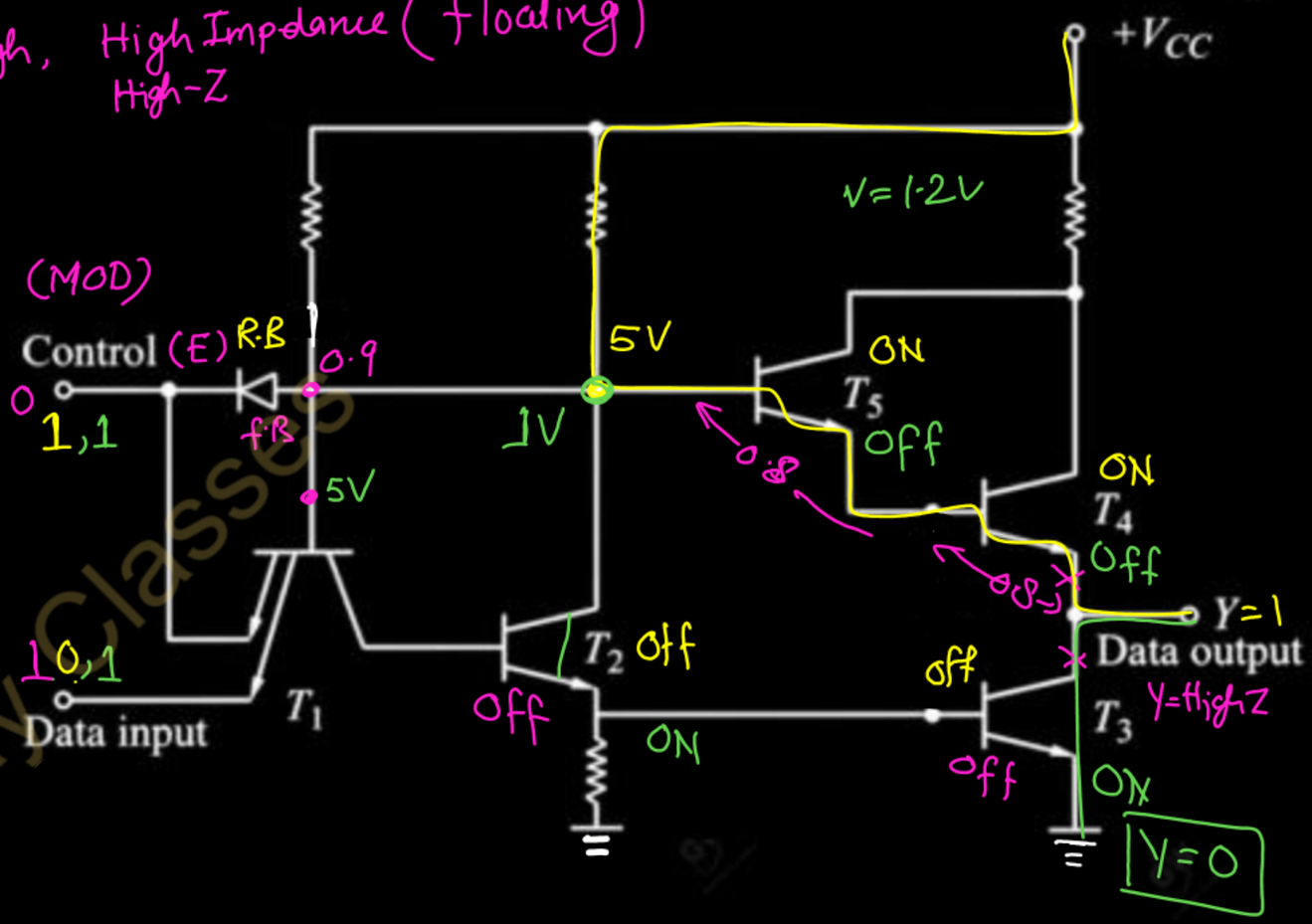
Gateway Classes

3. Tri-state gate output

Y = 0, 1
Low, high, High Impedance (floating)
High-Z

This configuration allows the output to effectively "disconnect" from the circuit, acting like an open switch. This is essential for computers where many devices share a single data wire (a Bus).

A tri-state output combines the benefits of both totem-pole output and open-collector output. Three states can be seen for the circuit with Tri-state output.

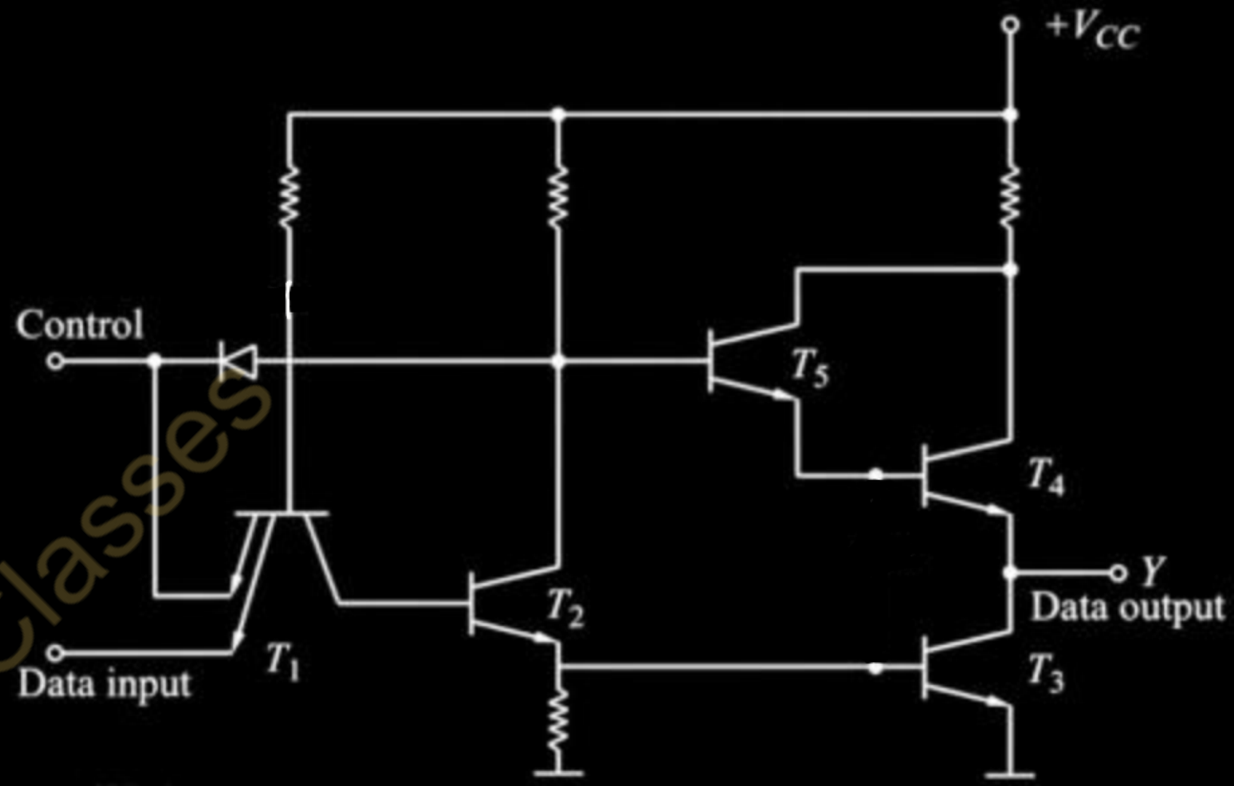


Gateway Classes

- Such circuits have an extra control input. If the control input is 1 the normal NAND operation is seen.
- When control input is 1 and all inputs are high, ***logic 0*** is seen.
- When control input is 1 and one of the inputs or all the inputs are 0, ***logic 1*** is seen.
- A ***high impedance*** also called the open-circuit state is seen when the control input is 0. In this case, the circuit behaves as if the output is disabled.

3. Tri-state gate output

- When control state C is HIGH and any input is LOW: Transistor T1 is ON, transistors T2 and T3 are OFF and transistors T4 and T5 are ON. The output is at a HIGH level.
- When control state C is HIGH and both inputs are HIGH: Transistor T1 is OFF, transistors T2 and T3 are ON and transistors T4 and T5 are OFF. The output is at a LOW level.



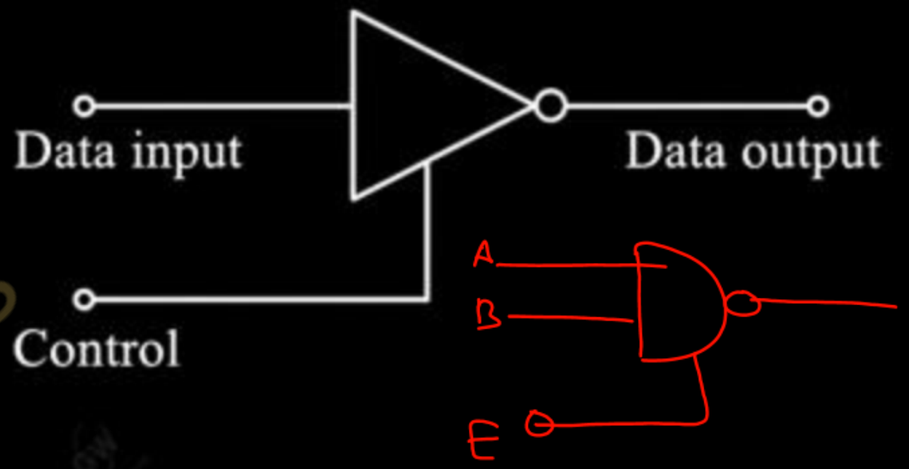
- When control state C is LOW: Irrespective of any input, transistor 1 is ON and all other transistors are OFF. The circuit is at HIGH impedance state.
- When control input is HIGH the circuit behaves similar to the totem-pole output circuit.
- When control input is LOW the circuit output is open-circuited.

Gateway Classes

3. Tri-state gate output (INVERTER)

AKTU 2024-25

- With E = 1, the circuit operates as a normal INVERTER because the high input at E has no effect on transistor Q1 or diode D2. In this enabled condition the output is simply the inverse of logic input



DATA INPUT	CONTROL INPUT(E)	OUTPUT
0	0	HIGH- Z
1	0	HIGH-Z
0	1	1
1	1	0

Gateway Classes

Advantages of Tri-State Gate Output

- Allows multiple devices to share a common bus.
- Eliminates short-circuit conflicts between logic drivers
- Enables bus-oriented system design
- Provides better expandability
- Reduces wiring complexity
- Improves system reliability and performance
- Supports controlled access using enable signal

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