AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-3 Lec-4



Avinash Sir

Today's target

- Shift Registers
- Bidirectional Shift Registers
- Universal Shift Registers
- PYQ

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

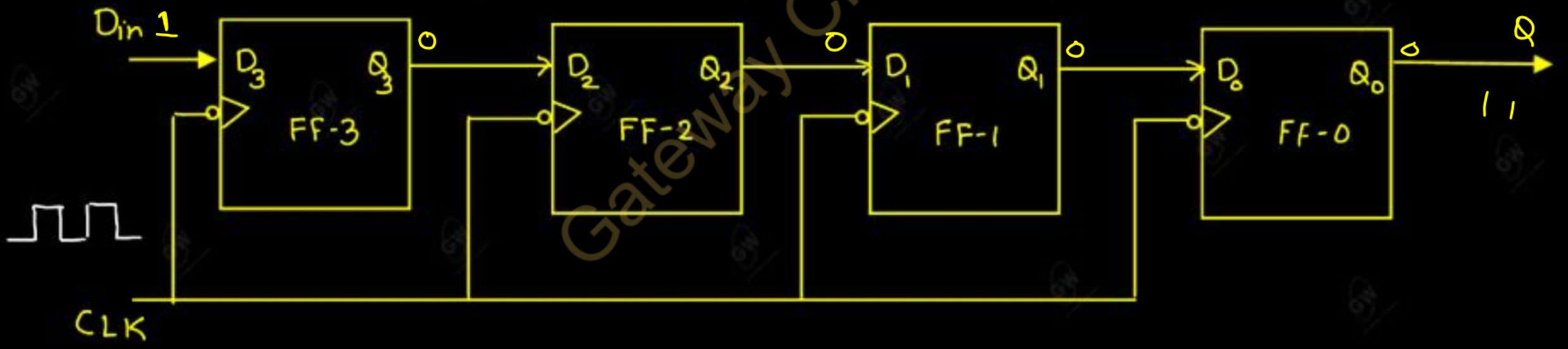
Shift Registers

- A Flip-flop is a 1 bit memory cell which can be used for storing the digital data. To increase the storage capacity in terms of number of bits, you can use a group of flip-flops. Such a group of flip-flops is known as a Register. The n-bit register will consist of n number of flip-flop(s) and it is capable of storing an n-bit word.
- A shift register is a type of register that allows such data transfers. Shift register has 4 modes of operations.
  - Serial-in serial-out SISO
  - Serial-in parallel-out SIPO
  - Parallel-in serial-out PISO
  - Parallel-in parallel-out PIPO

Gateway Classes

Serial-in serial-out (SISO)

Let all the flip-flops be initially in the reset condition i.e. Q3 = Q2 = Q1 = Q0 = 0. If an entry of a four-bit binary number 1 1 1 1 is made into the register, this number should be applied to D_{in} bit with the LSB bit applied first. The D input of FF-3 i.e. D3 is connected to serial data input D_{in}. The output of FF-3 i.e. Q3 is connected to the input of the next flip-flop i.e. D2, and so on.



Gateway Classes

- On the first falling edge of the clock, the FF-3 is set, and stored word in the register is Q3 Q2 Q1 Q0 = 1000.
- Apply the next bit to Din. So Din = 1. As soon as the next negative edge of the clock gets triggered, FF-2 will set and the stored word change to Q3 Q2 Q1 Q0 = 1100.
- Apply the next bit to be stored i.e. 1 to Din. Apply the clock pulse. As soon as the third negative clock edge gets triggered, FF-1 will be set and output will get modified to Q3 Q2 Q1 Q0 = 1110.
- Similarly with Din = 1 and with the fourth negative clock edge arriving, the stored word in the register is Q3 Q2 Q1 Q0 = 1111.

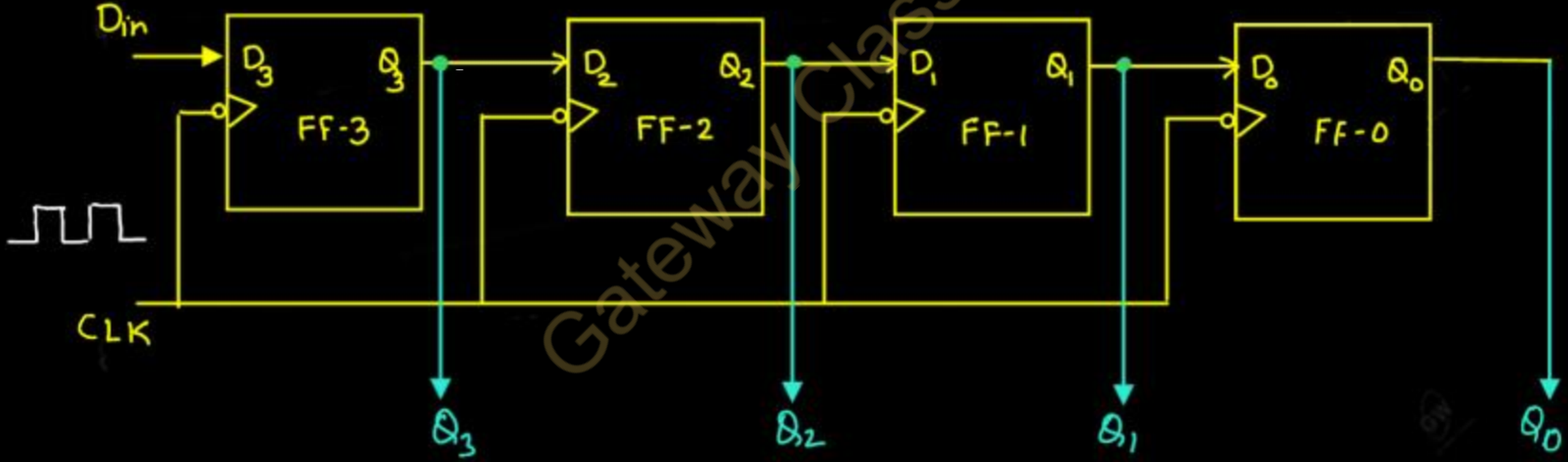
CLK	$D_{in}=Q_3$	$Q_3=D_2$	$Q_2=D_1$	$Q_1=D_0$	Q_0
X	–	0	0	0	0
1 ↓	1 →	1	0	0	0
2 ↓	1 →	1	1	0	0
3 ↓	1 →	1	1	1	0
↓	1 →	1	1	1	1

Direction of data travel →

Gateway Classes

Serial-in parallel-out (SIPO)

- In such types of operations, the data is entered serially and taken out in parallel fashion.
- Data is loaded bit-by-bit. The output(s) are disabled as long as the data is loading.
- As the data loading gets completed, all flip-flops contain their required data. The output(s) are enabled so that all the loaded data is made available over all the output lines at the same time.



Gateway Classes

- 4 clock cycles are required to load a four-bit word. Hence the speed of operation of SIPO mode is the same as that of the SISO mode.

Parallel-in serial-out

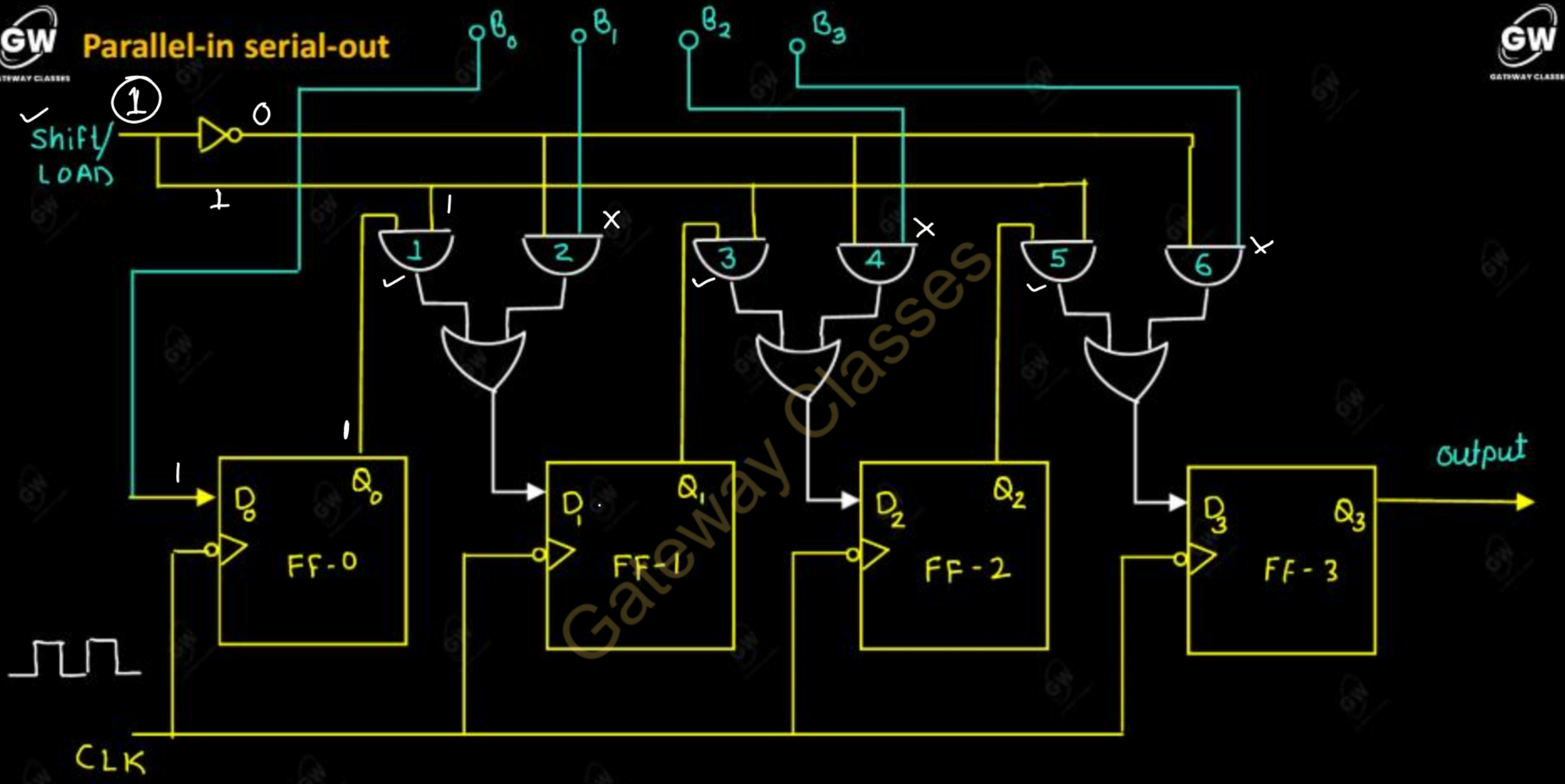
- Data bits enter in a parallel fashion.
- The circuit, shown below, is a four-bit parallel-in serial-out register.
- Output of the previous flip Flop is connected to the input of the next one via a combinational circuit.
- The binary input data bits B0, B1, B2, B3 are applied through the same combinational logic circuit.
- There are two modes in which this circuit can work, namely - shift mode and load mode.

Load mode:- When the shift/load bar line is low (0), the AND gates 2, 4 and 6 become active, and they will pass B_1, B_2, B_3 bits to the corresponding flip-flops. On –ve edge of the clock, the binary inputs B_0, B_1, B_2, B_3 will get loaded into the corresponding flip-flops. Thus, the parallel loading takes place.

Shift mode:- When the shift/load bar line is high (1), the AND gates 2, 4 and 6 become inactive. AND gates 1,3 and 5 become active. Therefore the shifting of data takes place from left-to-right bit-by-bit on the application of clock pulses. Thus, the parallel-in serial-out operation takes place.

Gateway Classes

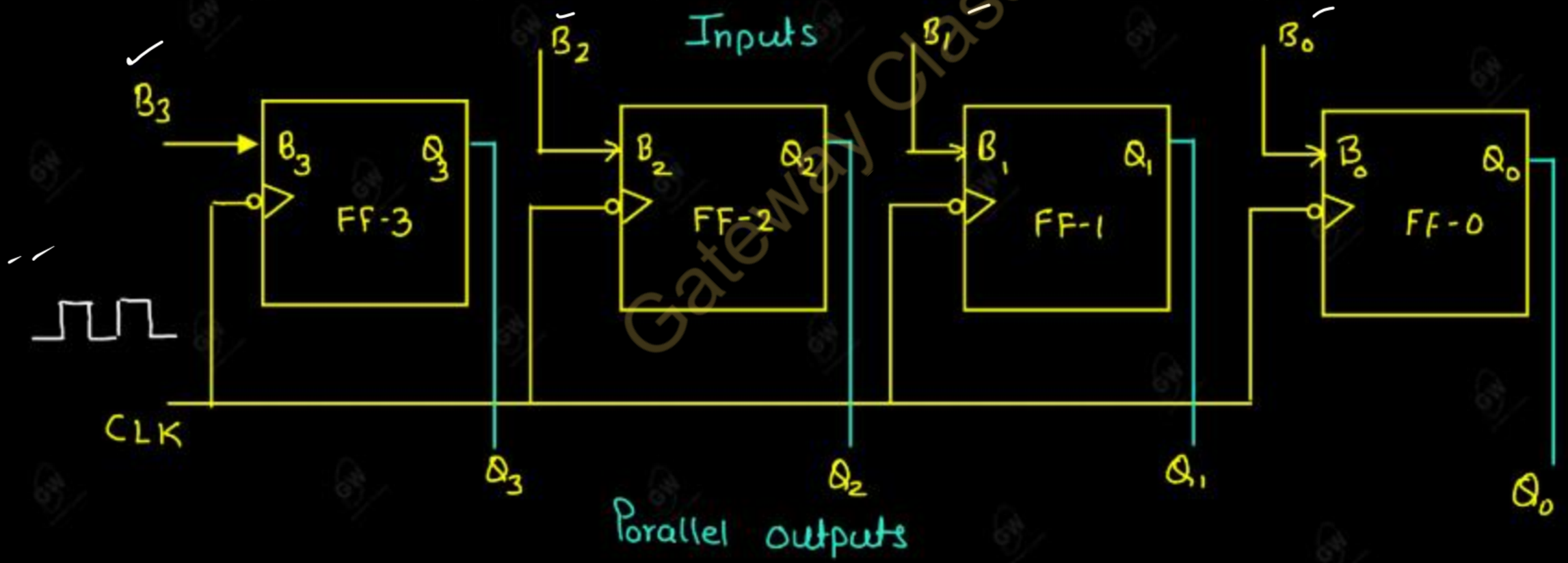
Parallel-in serial-out



Gateway Classes

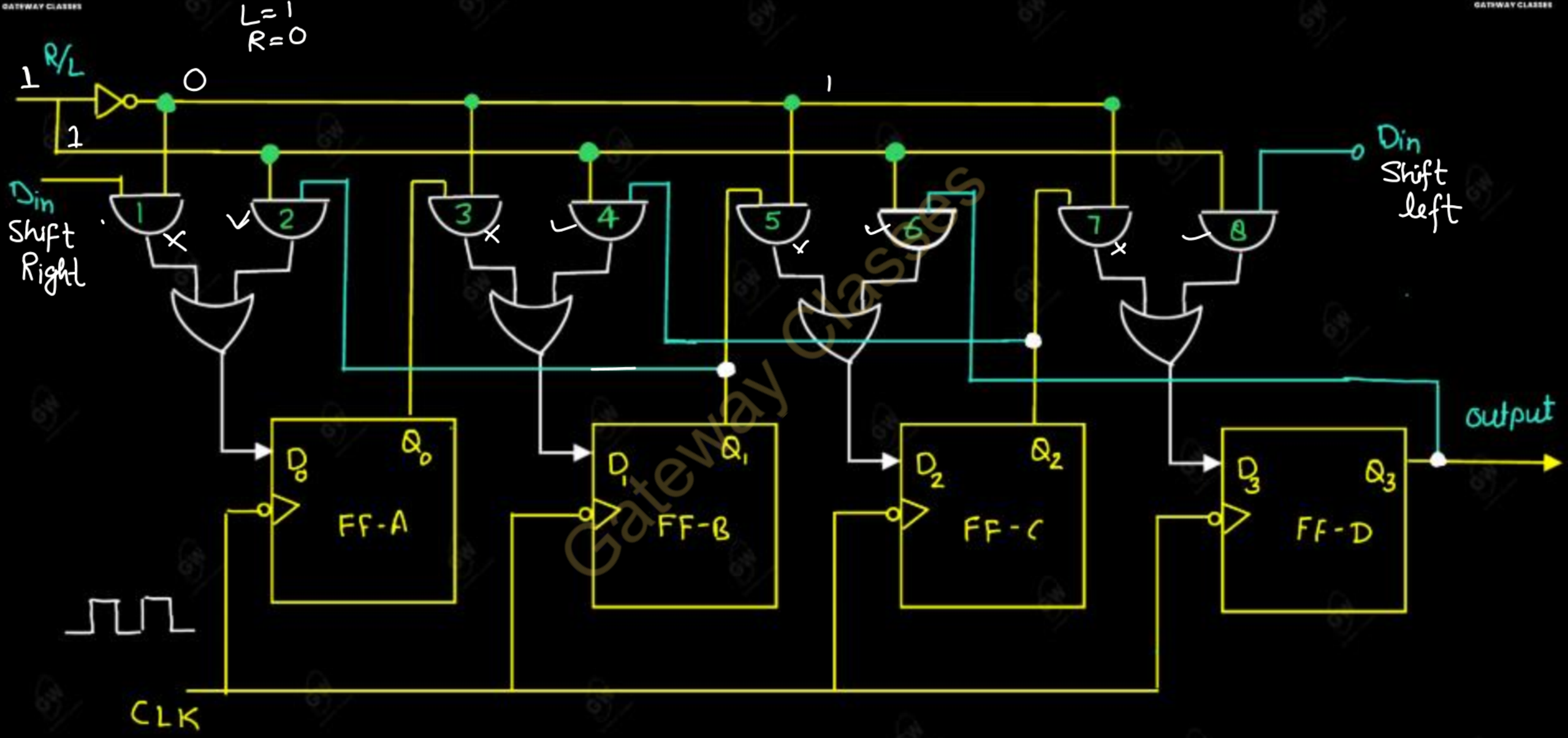
Parallel-in parallel-out

Here, the 4-bit binary data inputs B0, B1, B2, B3 are applied to the data inputs D0, D1, D2, D3, respectively, of the four flip-flops. When a negative edge of the clock is triggered, then the flip-flops get loaded with the input binary bits simultaneously. The loaded bits appear at the output side, simultaneously, as well. Only the clock pulse is essential to load all the binary bits.



Gateway Classes

Bidirectional Shift Register



Gateway Classes

Bidirectional Shift Register

Case 1: Shift-Right Operation

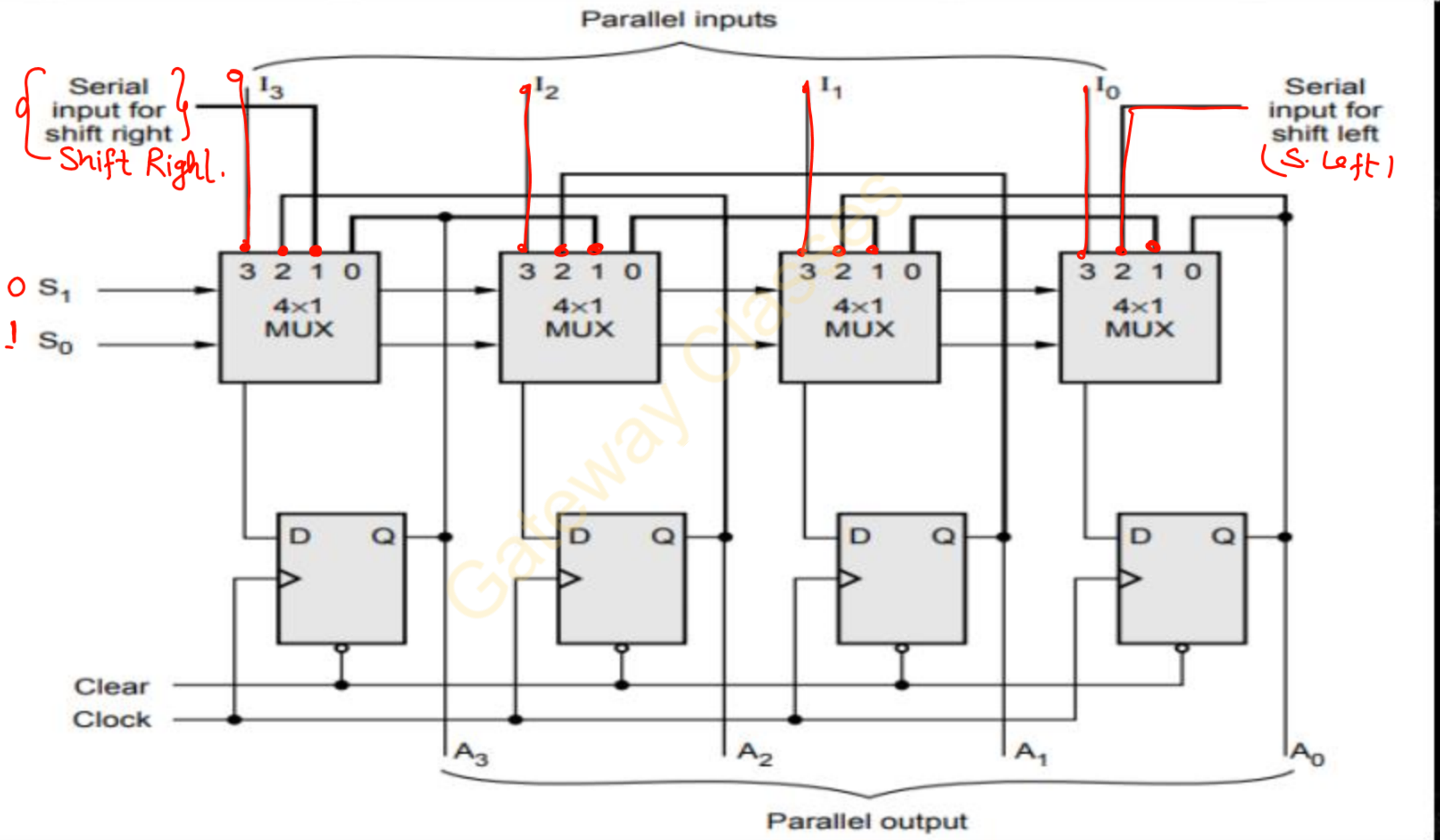
When the control signal R/L' is HIGH, then the AND gates 1, 3, 5, and 7 are enabled, and the AND gates 2, 4, 6, and 8 are disabled. The output of the flip-flop A is connected to the input of the flip-flop B, the output of the flip-flop B is connected to the input of the flip-flop C, and the output of the flip-flop C is connected to the input of the flip-flop D. Hence, when a clock signal occurs, the data bits are shifted one place to the right.

Case 2: Shift-Left Operation

When the control signal R/L' is LOW, then the AND gates 2, 4, 6, and 8 are enabled, and the AND gates 1, 3, 5, and 7 are disabled. The output Q of each flip-flop connected to the D input of the following flip-flop. Thus, when a clock signal occurs, the data bits are shifted one place to the left.

Gateway Classes

S0 S1
0 0 → NC
0 1 → SR
1 0 - S.L
1 1 -
Parallel loading



Gateway Classes

Universal Shift Register

- If the register has both shifts (right shift and left shift) and parallel load capabilities, it is referred to as universal shift register.
- The four multiplexers have two common selection inputs S1 and S0, and they select appropriate input for D flip-flop.
- When $S_1S_0 = 00$, I_0 is selected ,no change in the register value.
- When $S_1S_0 = 01$, I_1 is selected, operates as a right shift register.
- When $S_1S_0 = 10$, I_2 is selected, operates as a left shift register.
- Finally, when $S_1S_0 = 11$, it is a parallel load operation.

Mode control		Register operation
S_1	S_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Mode control and register operation

Gateway Classes

Gateway Classes

Empowering Learners, Transforming Futures

GATEWAY CLASSES

Thank You

Gateway Classes

GET IT ON Google Play

Download on the App Store

Helpline No- 7819 0058 53