AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-2 Lec-7



Avinash Sir

Today's target

- Circuit realization using De Multiplexers
- PYQ
- DPP

Gateway Classes

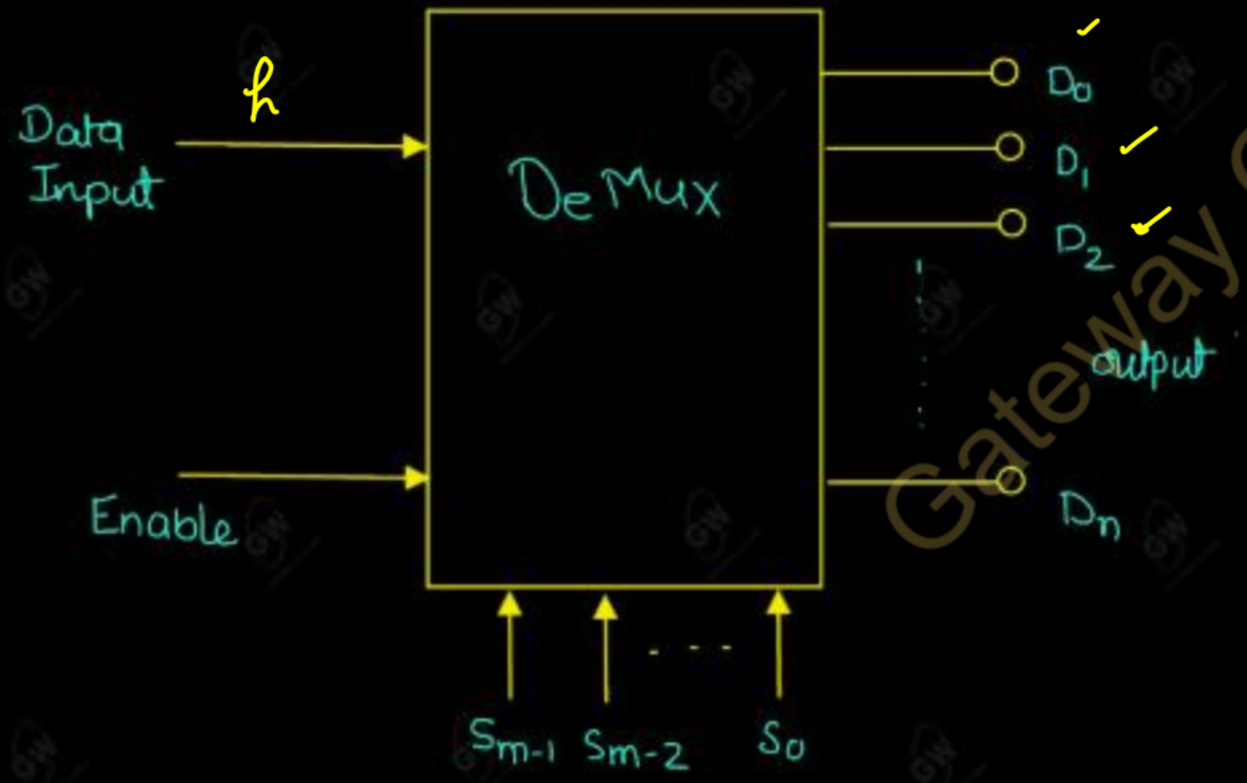
UNIT-2 : Combinational circuits:

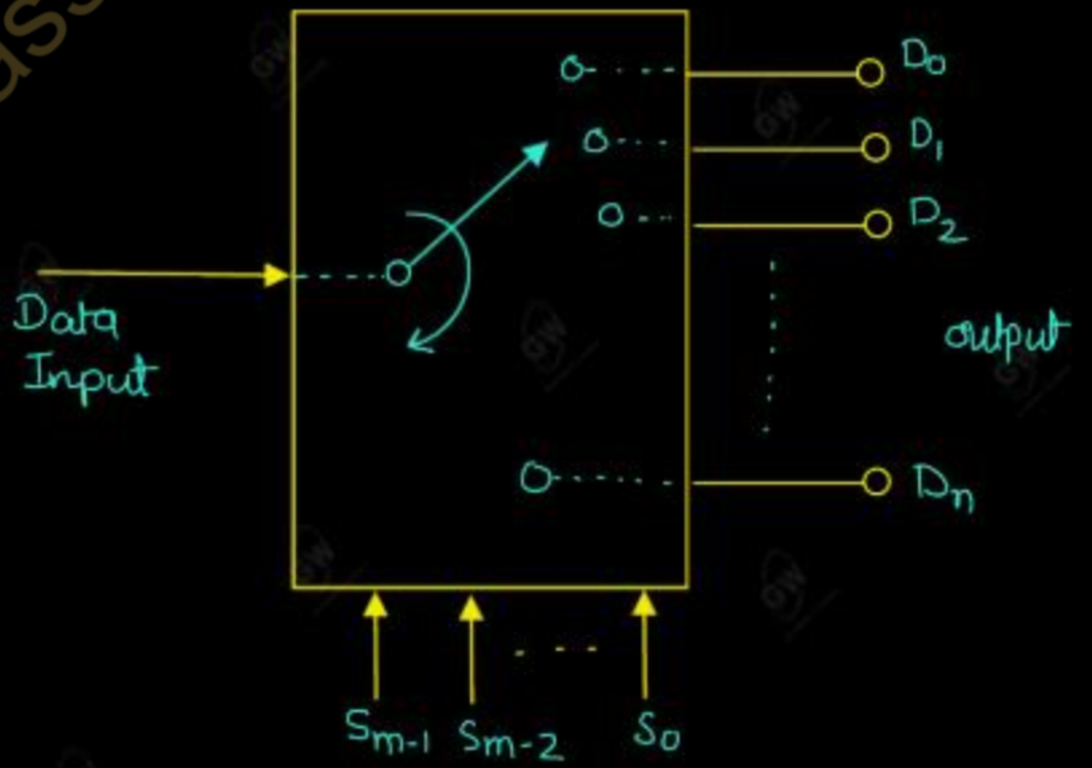
- Analysis and Design of combinational circuits
- MSI devices like comparators, multiplexers, demultiplexers, encoder, decoder,
- circuit realization using Multiplexers and decoders, half and full adders, subtractors, serial and parallel adders, BCD adder, barrel shifter and ALU.

Gateway Classes

Demultiplexer

A demultiplexer performs the reverse operation of a multiplexer i.e. it receives one input and distributes it over several outputs. It has only one input, n outputs, m select input. At a time only one output line is selected by the select lines and the input is transmitted to the selected output line.





Gateway Classes

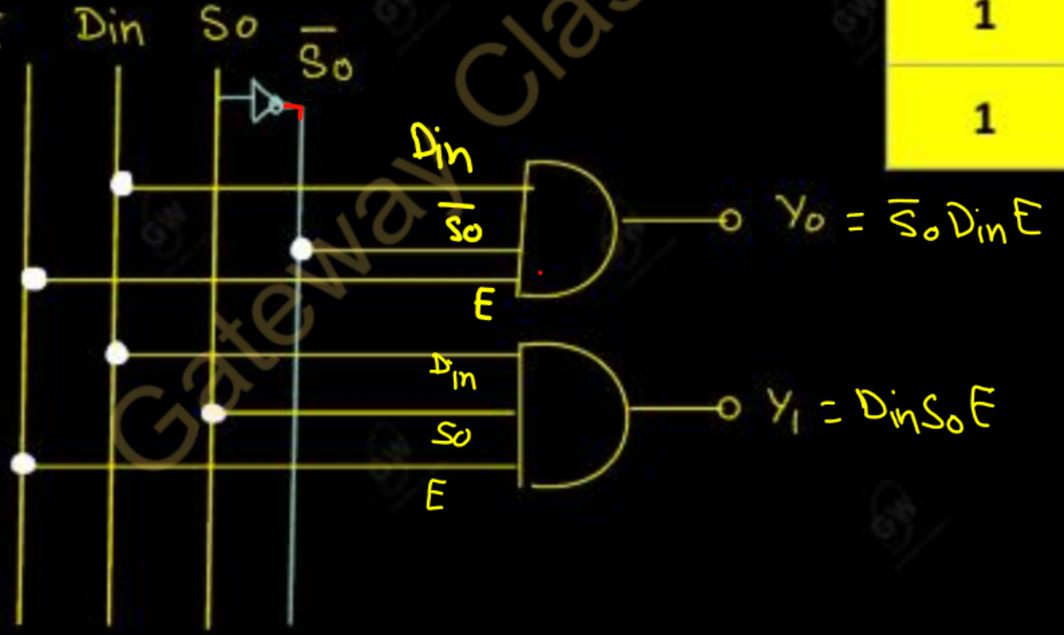
1 : 2 Demultiplexer



$\bar{S}_0$

2 → 1 → S.L.

Enable	INPUTS	OUTPUTS	
E	S0	Y1	Y0
0	X	0	0
1	0	0	Din
1	1	Din	0



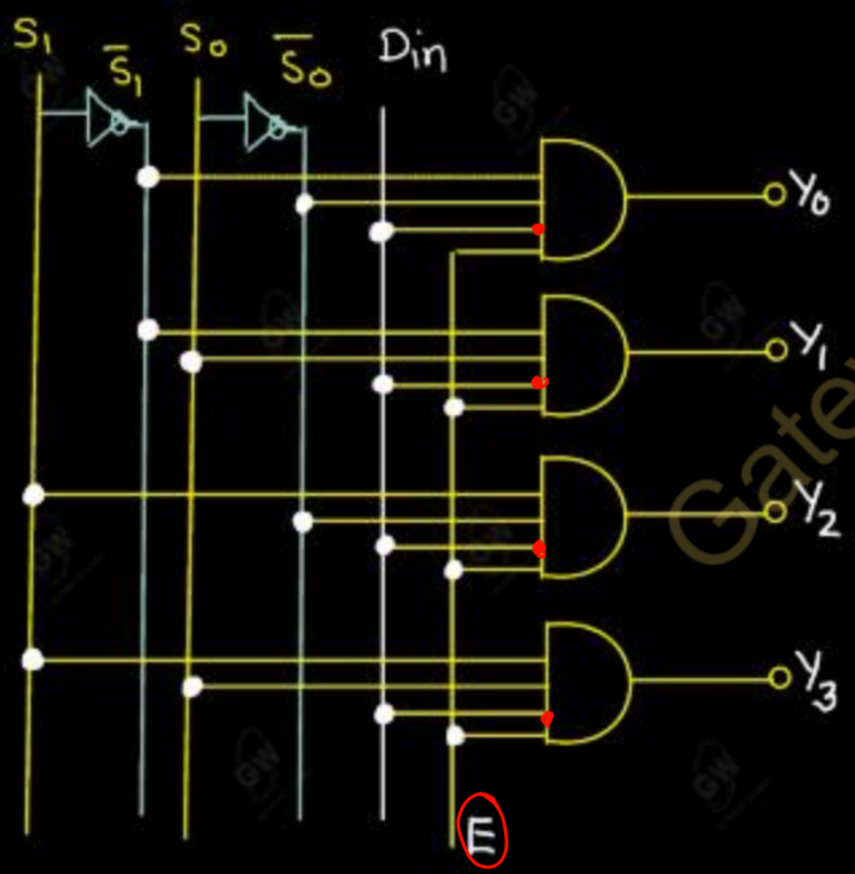
$Y_0 = \bar{S}_0 Din E$

$Y_1 = Din S_0 E$

Gateway Classes

1 : 4 Demultiplexer





Enable	INPUTS	Select Line		Output				
E	Din	S1	S0	Y0	Y1	Y2	Y3	
1	0	0	0	0	0	0	0	$\bar{S}_1\bar{S}_0 D_{in}$ Y_0
1	1	0	0	1	0	0	0	
1	0	0	1	0	0	0	0	$\bar{S}_1 S_0 D_{in}$ Y_1
1	1	0	1	0	1	0	0	
1	0	1	0	0	0	0	0	$S_1\bar{S}_0 D_{in}$ Y_2
1	1	1	0	0	0	1	0	
1	0	1	1	0	0	0	0	$S_1 S_0 D_{in}$ Y_3
1	1	1	1	0	0	0	1	

Gateway Classes

1 : 8 Demultiplexer

$2^3 \rightarrow$ S.L.

$$Y_0 = \bar{S}_2\bar{S}_1\bar{S}_0 Din$$
$$Y_1 = \bar{S}_2\bar{S}_1 S_0 Din$$
$$Y_2 = \bar{S}_2 S_1\bar{S}_0 Din$$
$$Y_3 = \bar{S}_2 S_1 S_0 Din$$
$$Y_4 = S_2\bar{S}_1\bar{S}_0 Din$$
$$Y_5 = S_2\bar{S}_1 S_0 Din$$
$$Y_6 = S_2 S_1\bar{S}_0 Din$$
$$Y_7 = S_2 S_1 S_0 Din$$

En.	I/P	Select		Output								
E	S2	S1	S0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
0	X	X	X	0	0	0	0	0	0	0	0	
1	0	0	0	D_{in}	0	0	0	0	0	0	0	$\bar{S}_2\bar{S}_1\bar{S}_0 D_{in}$
1	0	0	1	0	D_{in}	0	0	0	0	0	0	$\bar{S}_2\bar{S}_1 S_0 D_{in}$
1	0	1	0	0	0	D_{in}	0	0	0	0	0	$\bar{S}_2 S_1\bar{S}_0 D_{in}$
1	0	1	1	0	0	0	D_{in}	0	0	0	0	$\bar{S}_2 S_1 S_0 D_{in}$
1	1	0	0	0	0	0	0	D_{in}	0	0	0	$S_2\bar{S}_1\bar{S}_0 D_{in}$
1	1	0	1	0	0	0	0	0	D_{in}	0	0	$S_2\bar{S}_1 S_0 D_{in}$
1	1	1	0	0	0	0	0	0	0	D_{in}	0	$S_2 S_1\bar{S}_0 D_{in}$
1	1	1	1	0	0	0	0	0	0	0	D_{in}	$S_2 S_1 S_0 D_{in}$

Gateway Classes

1 : 8 Demultiplexer

$Y_0 = \bar{S}_2 \bar{S}_1 \bar{S}_0 Din$

$Y_1 = \bar{S}_2 \bar{S}_1 S_0 Din$

$Y_2 = \bar{S}_2 S_1 \bar{S}_0 Din$

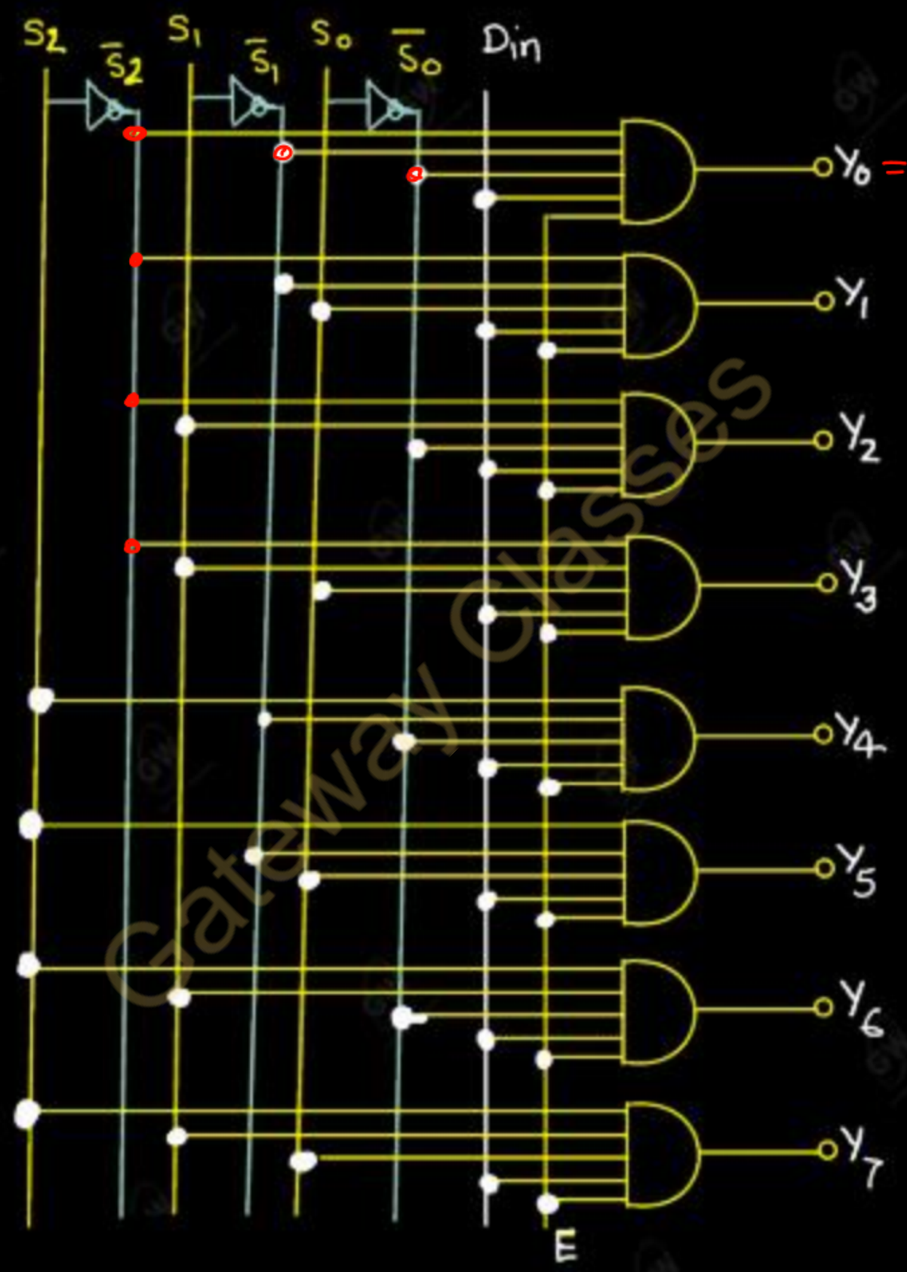
$Y_3 = \bar{S}_2 S_1 S_0 Din$

$Y_4 = S_2 \bar{S}_1 \bar{S}_0 Din$

$Y_5 = S_2 \bar{S}_1 S_0 Din$

$Y_6 = S_2 S_1 \bar{S}_0 Din$

$Y_7 = S_2 S_1 S_0 Din$



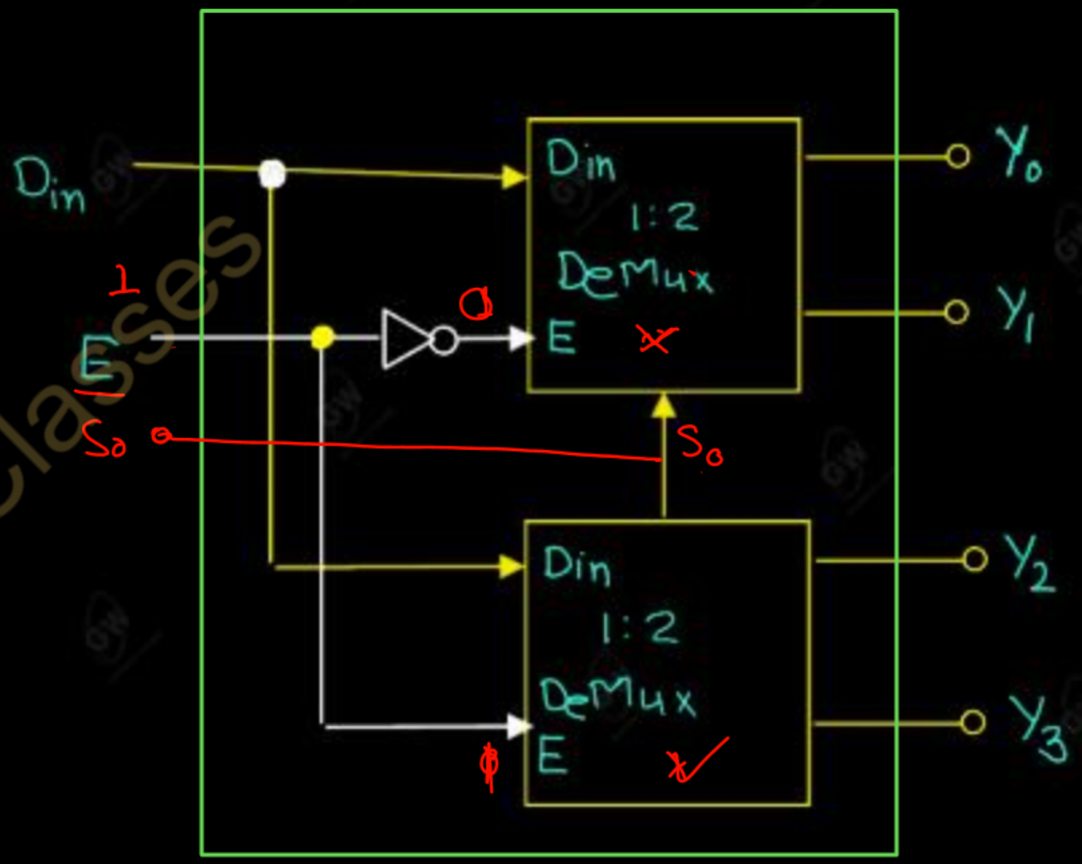
$Y_0 = \bar{S}_2 \bar{S}_1 \bar{S}_0 Din\, E$

Gateway Classes

Q.1 . Design 1: 4 line Demultiplexer using 1: 2 Demux.

Truth Table

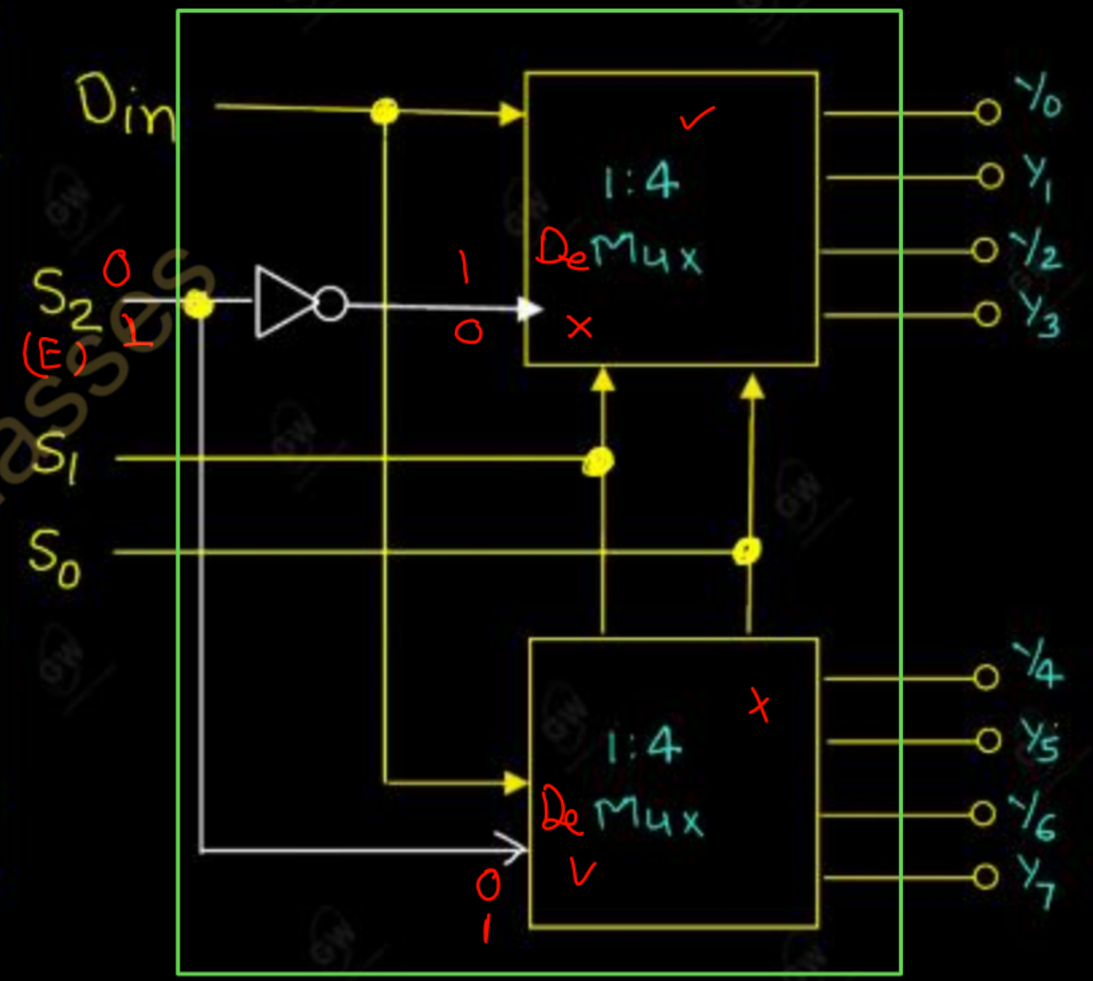
ENABLE	Select I/P		output				
	S_1	S_0	Y_0	Y_1	Y_2	Y_3	
0	0	0	D_{in}	0	0	0	Demux 1 Activated
0	0	1	0	D_{in}	0	0	Demux 1 Activated
1	1	0	0	0	D_{in}	0	Demux 2 Activated
1	1	1	0	0	0	D_{in}	Demux 2 Activated



Gateway Classes

Q.3 . Design 1 : 8 line Demultiplexer using 1: 4 Demux.

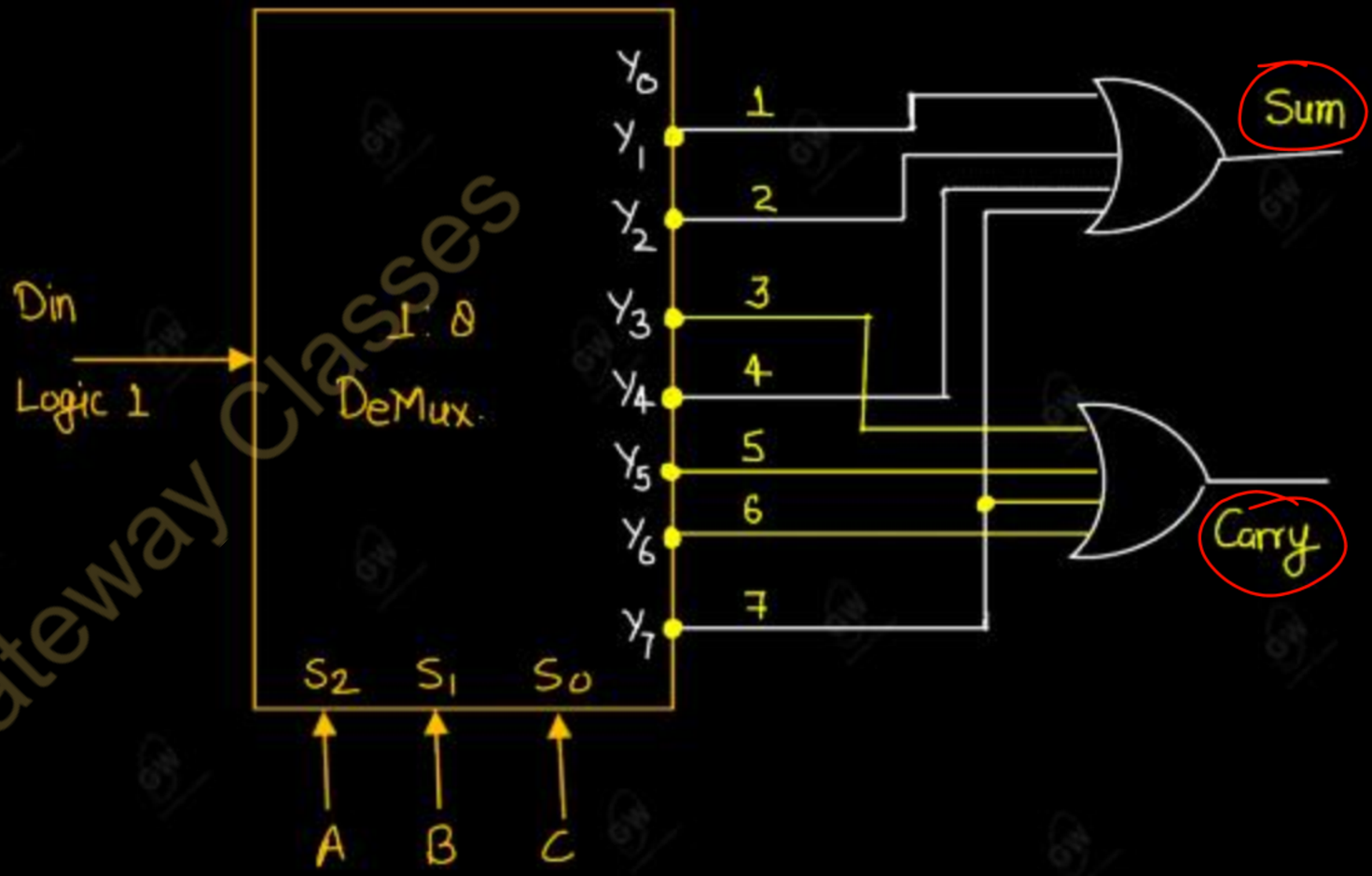
Select Inputs			Outputs							
S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	Din	0	0	0	0	0	0	0
0	0	1	0	Din	0	0	0	0	0	0
0	1	0	0	0	Din	0	0	0	0	0
0	1	1	0	0	0	Din	0	0	0	0
1	0	0	0	0	0	0	Din	0	0	0
1	0	1	0	0	0	0	0	Din	0	0
1	1	0	0	0	0	0	0	0	Din	0
1	1	1	0	0	0	0	0	0	0	Din



Gateway Classes

Q.4 . Implement a full adder using Demultiplexer.

	INPUTS			OUTPUTS	
	A	B	C_{in}	Sum (S)	Carry out (C)
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1



$Sum = \Sigma m(1,2,4,7)$

$Carry = \Sigma m(3,5,6,7)$

Gateway Classes

DPP

Q.1 . Design 1: 32 line Demultiplexer using 1: 4 Demultiplexer.

Q.2 Implement the following expression using a multiplexer:

$F(A,B,C) = \Sigma m\ (0,2,3,6,8,\ 9\ ,\ 11,12,\ 14)$

Q.3 Implement the following function using a 4 to 16 line decoder:

$F = \Sigma m\ (1,2,4,7,8,\ 11,12,\ 13)$

Gateway Classes

Gateway Classes

Empowering Learners, Transforming Futures

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Thank You

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