AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-3 Lec-5



Avinash Sir

Today's target

- Ripple and synchronous counters,
- Ring counter
- Johnson counter
- PYQ

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

UNIT-3

- **Sequential logic design:** Building blocks like S-R, JK and Master-Slave JK FF, D FF, T FF, edge triggered FF, Flip flop conversion.
- **Applications of Flip Flops:** ripple and synchronous counters, Ring counter, Johnson counter.
- **shift registers:** SISO, SIPO, PISO, PIPO, Bidirectional shift register, Universal shift register.
- **Finite state machines:** Mealy and Moore machines, State diagrams, state reduction, Analysis of clocked sequential circuits, Design of clocked sequential circuits.

Gateway Classes

Types of Counters

- 1. Asynchronous counter ⇒ Ripple counter, serial (or) series (up/down)
- 2. Synchronous counter ⇒ Parallel counter

Asynchronous → CLK Pulse to first ff.

Synchronous → CLK Pulse to all ff.

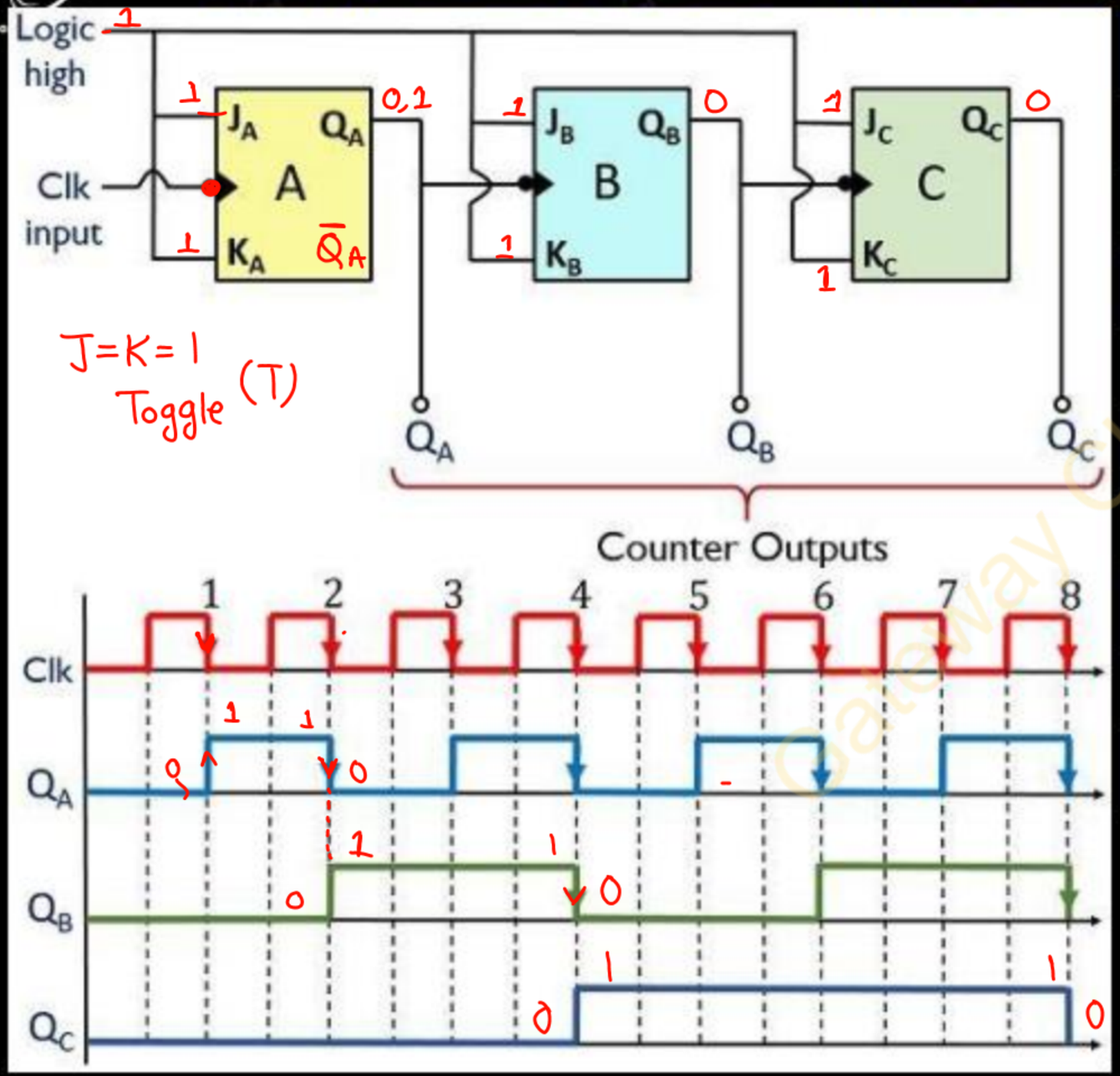
Gateway Classes

Synchronous Counter	Asynchronous Counter
Common clock applied to all flip flops.	main clock is only applied to the first flip flop and then for rest of flip flops the output of previous flip flop is taken as a clock.
Synchronous Counter is faster in operation	Asynchronous Counter is slower
Synchronous Counter is also called Parallel Counter.	Asynchronous Counter is also called Serial Counter.
designing as well implementation are complex due to increasing the number of states.	designing as well as implementation is very easy.
operate in any desired count sequence.	operate only in fixed count sequence (UP/DOWN).
propagation delay is less.	there is high propagation delay.

Gateway Classes

3-Bit Asynchronous counter ⇒ Ripple counter, serial (or) series

JK, T

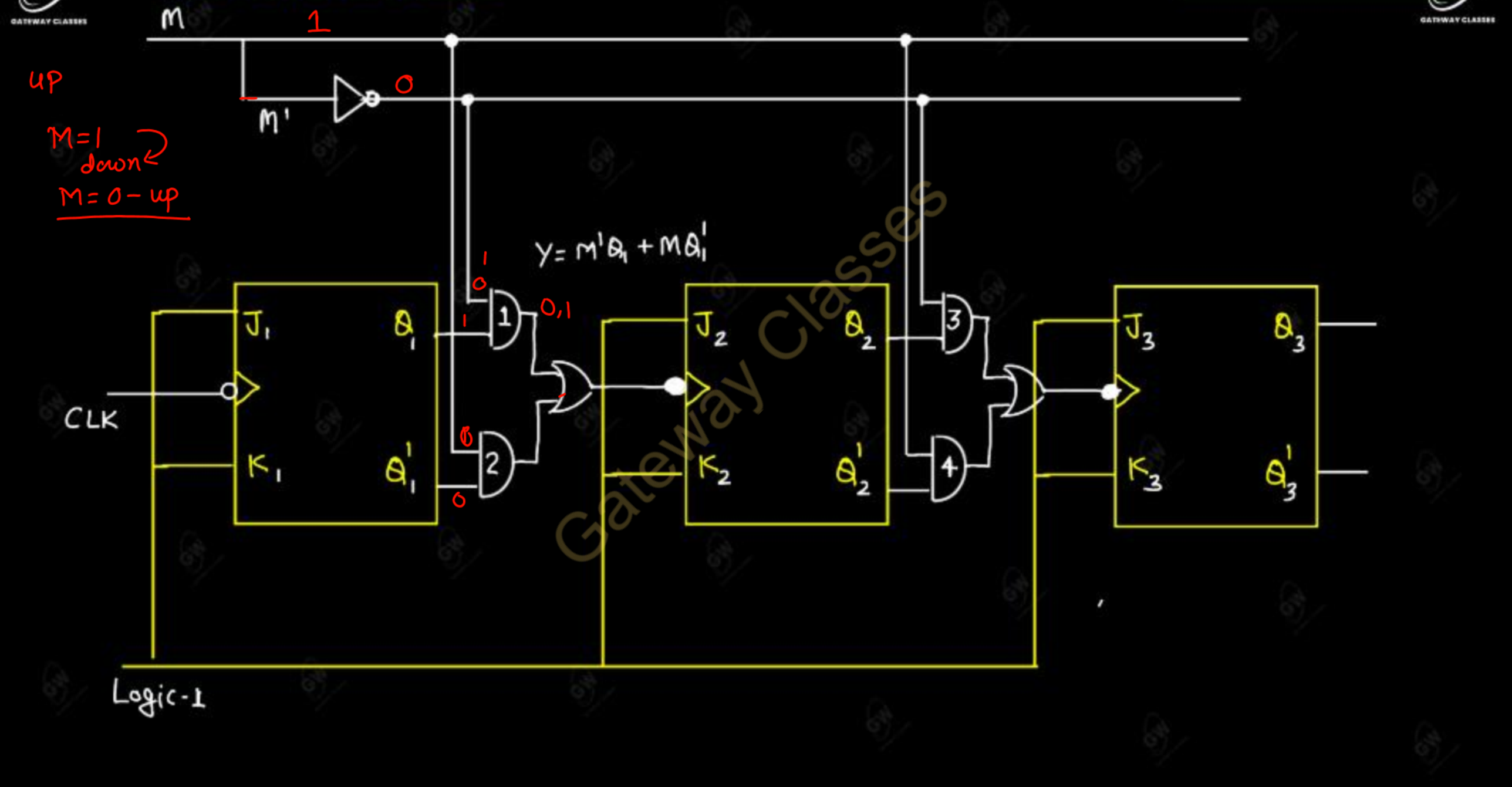


Clock	Qc	QB	QA	Decimal
Intiial	0	0	0	0
1st falling Edge	0	0	1	1
2nd falling Edge	0	1	0	2
3rd falling Edge	0	1	1	3
4th falling Edge	1	0	0	4
5th falling Edge	1	0	1	5
6th falling Edge	1	1	0	6
7th falling Edge	1	1	1	7
8th falling Edge	0	0	0	0

Gateway Classes

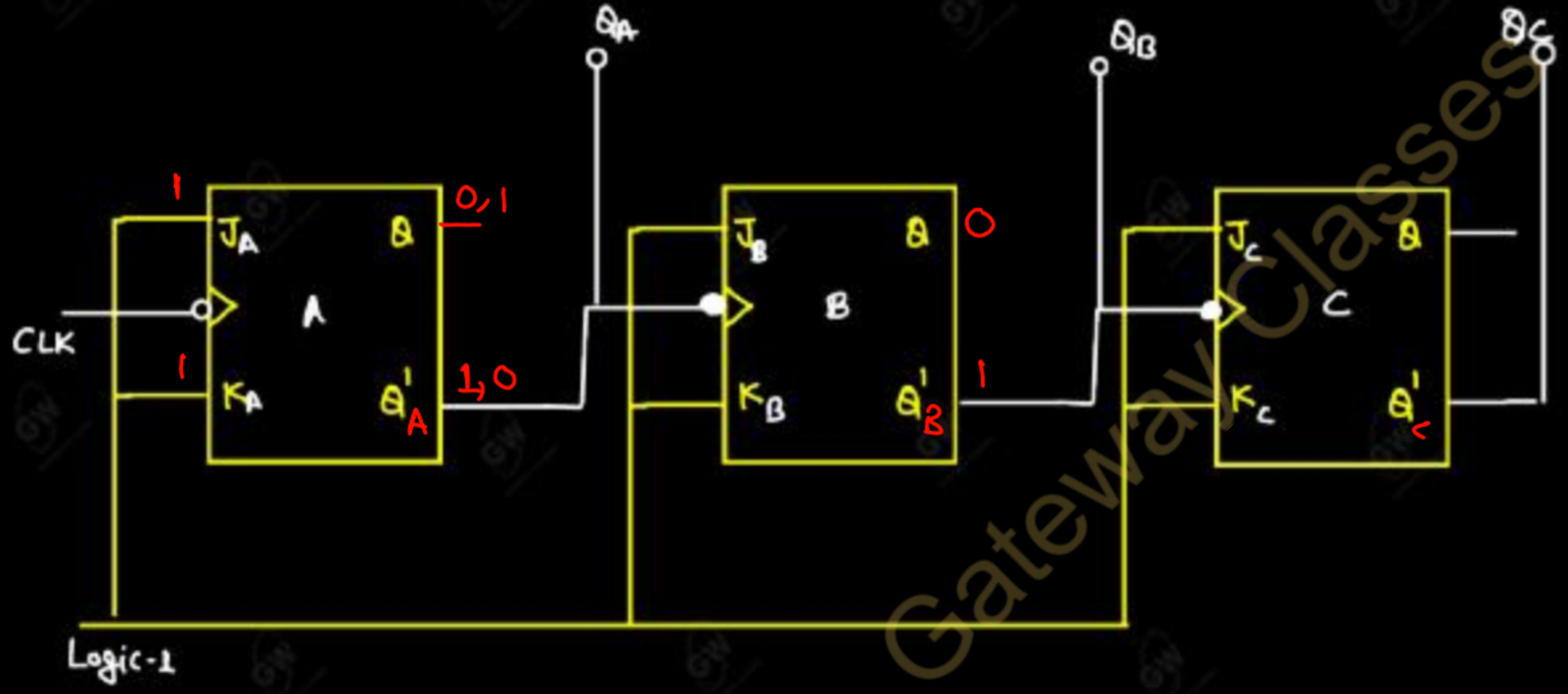
3 bit UP/Down Counter

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Gateway Classes

Down Counter



CLK	Q_C	Q_B	Q_A	Dec.
1 ↓	1	1	1	7
2 ↓	1	1	0	6
3 ↓	1	0	1	5
4 ↓	1	0	0	4
5 ↓	0	1	1	3
6 ↓	0	1	0	2
7 ↓	0	0	1	1
8 ↓	0	0	0	0

Gateway Classes

4- Bit Synchronous Counter (UP)

0000 — 1111

n = 4

ff = 4

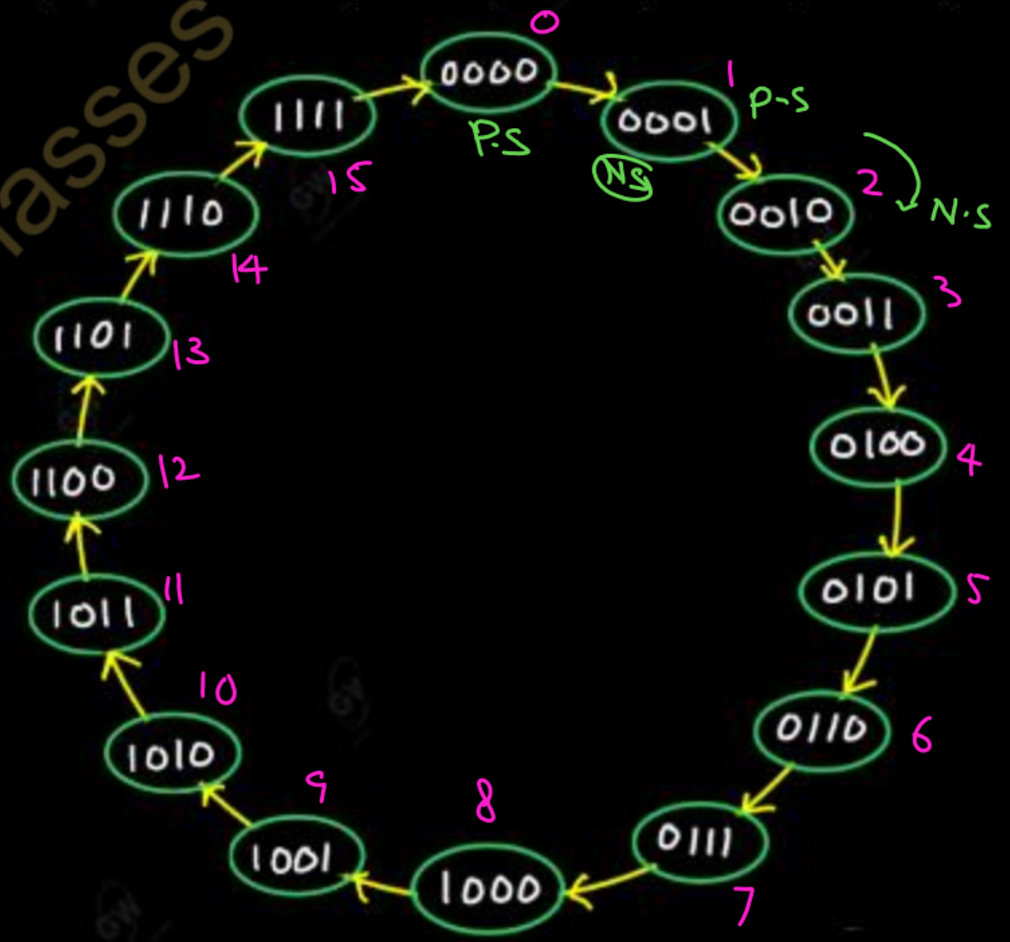
2^4 = 16 state

Step 1: Find the number of flip flops.

for a 4 bit counter, 4 flip flops(n=4) are needed

Number of states = $2^n = 2^4$ = 16states (0000, 0001, 0010,0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111)

Step 3: Draw state diagram for the counter.



Gateway Classes

Step 4: Obtain excitation table for the counter.

excitation table for Counter

CLK	Present state Q_D	Q_C	Q_B	Q_A	Next state Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A	
1	0	0	0	0	0	0	0	1	0	x	0	x	0	x	1	x	0
2	0	0	0	1	0	0	1	0	0	x	0	x	1	x	x	1	1
3	0	0	1	0	0	0	1	1	0	x	0	x	x	0	1	x	2
4	0	0	1	1	0	1	0	0	0	x	1	x	x	1	x	1	3
5	0	1	0	0	0	1	0	1	0	x	x	0	0	x	1	x	4
6	0	1	0	1	0	1	1	0	0	x	x	0	1	x	x	1	5
7	0	1	1	0	0	1	1	1	0	x	x	0	x	0	1	x	6
8	0	1	1	1	1	0	0	0	1	x	x	1	x	1	x	1	7
9	1	0	0	0	1	0	0	1	x	0	0	x	0	x	1	x	8
10	1	0	0	1	1	0	1	0	x	0	0	x	1	x	x	1	9
11	1	0	1	0	1	0	1	1	x	0	0	x	x	0	1	x	10
12	1	0	1	1	1	1	0	0	x	0	1	x	x	1	x	1	11
13	1	1	0	0	1	1	0	1	x	0	x	0	0	x	1	x	12
14	1	1	0	1	1	1	1	0	x	0	x	0	1	x	x	1	13
15	1	1	1	0	1	1	1	1	x	0	x	0	x	0	1	x	14
16	1	1	1	1	0	0	0	0	x	1	x	1	x	1	x	1	15

excitation table for JK flip flop

P.S Q_n	N.S Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

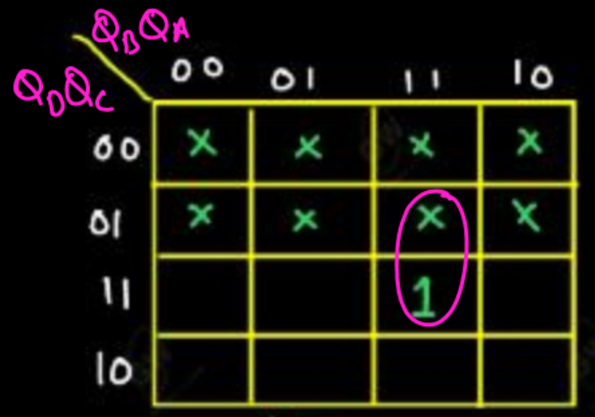
Gateway Classes

Step 5: Derive the flip flop input functions.

Using Karnaugh maps, the input functions for the 4 flip flops are derived.



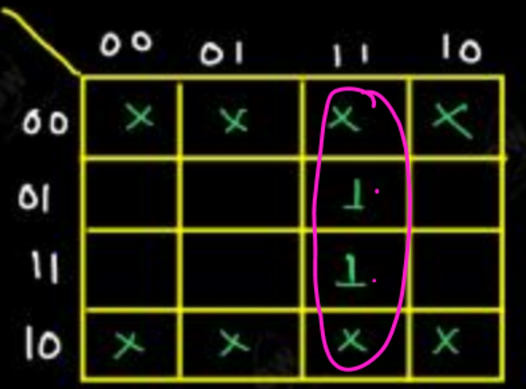
$J_D = Q_A Q_B Q_C$



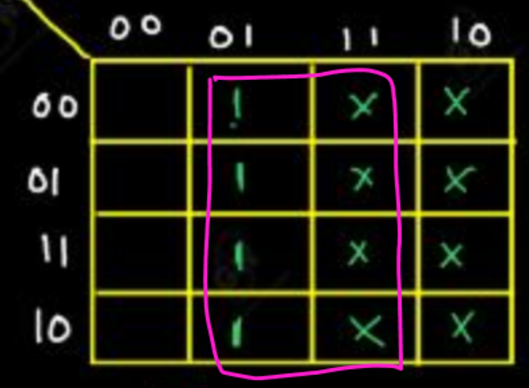
$K_D = Q_A Q_B Q_C$



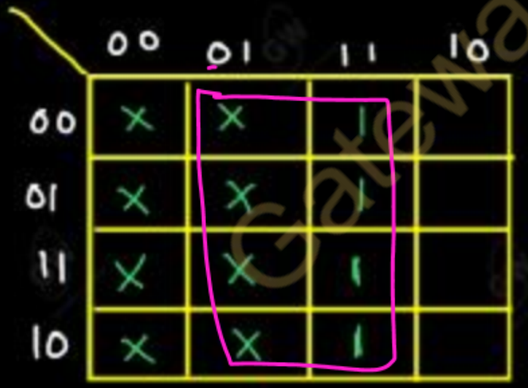
$J_C = Q_A Q_B$



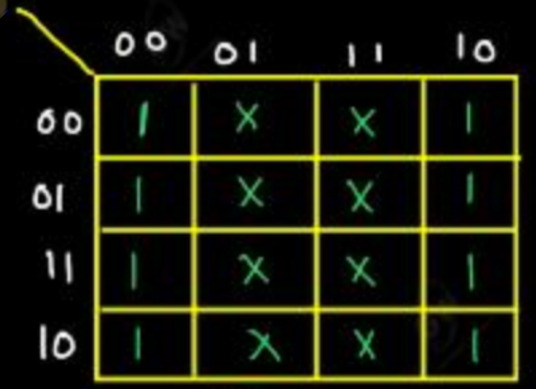
$K_C = Q_A Q_B$



$J_B = Q_A$



$K_B = Q_A$



$J_A = 1$

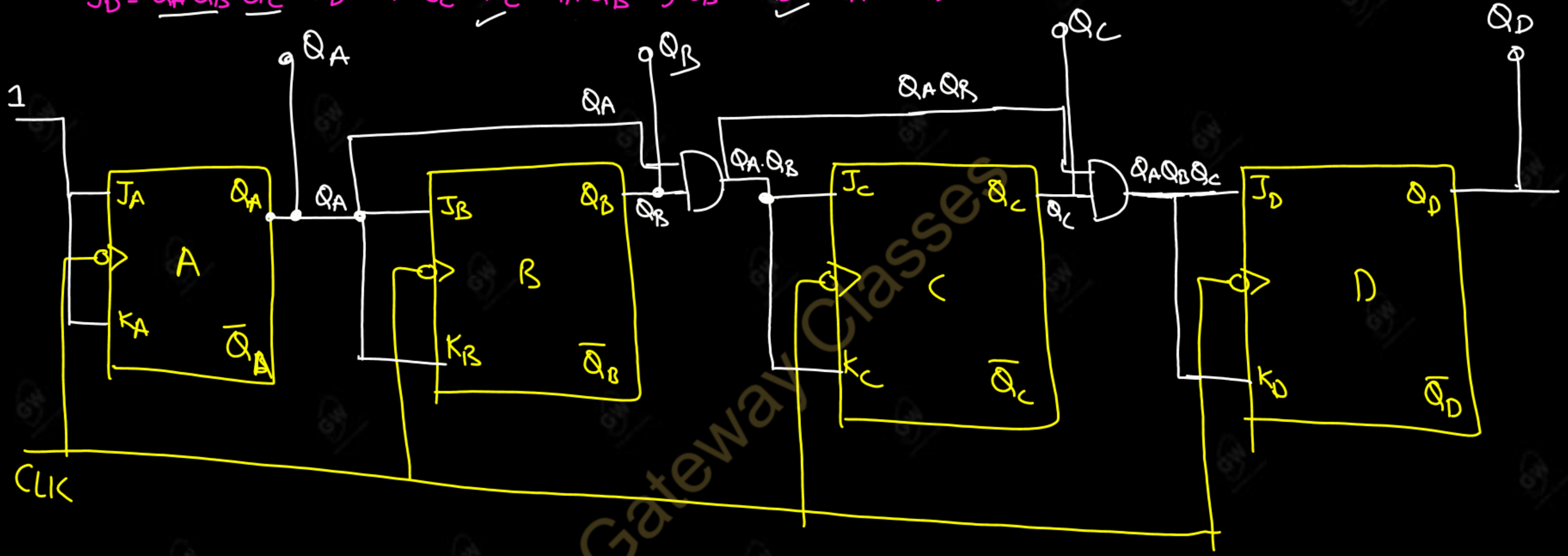


$K_A = 1$

Gateway Classes

Step 6: Draw the logic diagram of the counter.

$J_D = Q_A Q_B Q_C = K_D$, $J_C = K_C = Q_A Q_B$, $J_B = K_B = Q_A$, $J_A = K_A = 1$



Gateway Classes

3- Bit Synchronous Counter (UP)

$2^n = 8$

000 — 111 → 8 state

Step 1: Find the number of flip flops.

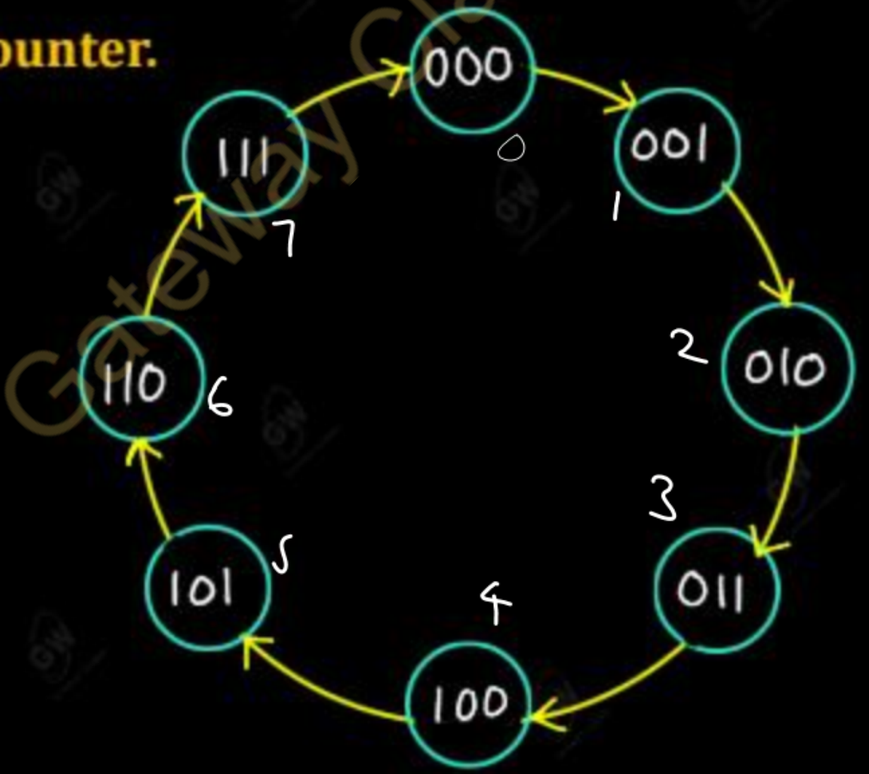
for a 3 bit counter, 3 flip flops(n=3) are needed

Number of states = $2^n = 2^3 = 8$ states(000, 001, 010, 011, 100, 101, 110, 111)

Step 2: Choose the type of flip flop.

Since the type of flip flop is given in the problem, let us use JK flip flops.

Step 3: Draw state diagram for the counter.



Gateway Classes

Step 4: Obtain excitation table for the counter.

excitation table for Counter

Clock	Present State			Next State			Flip flop Inputs					
	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
1	0	0	0	0	0	1	0	X	0	X	1	X
2	0	0	1	0	1	0	0	X	1	X	X	1
3	0	1	0	0	1	1	0	X	X	0	1	X
4	0	1	1	1	0	0	1	X	X	1	X	1
5	1	0	0	1	0	1	X	0	0	X	1	X
6	1	0	1	1	1	0	X	0	1	X	X	1
7	1	1	0	1	1	1	X	0	X	0	1	X
8	1	1	1	0	0	0	X	1	X	1	X	1

excitation table for JK flip flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 5: Derive the flip flop input functions.

Using Karnaugh maps, the input functions for the 3 flip flops are derived.

For J_C

Q_C \ Q_BQ_A	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_C = Q_BQ_A$ $Q_A \cdot Q_B = J_C$

For K_C

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	X	X
1	0	0	1	0

$K_C = Q_BQ_A$

For J_B

Q_C \ Q_BQ_A	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$J_B = Q_A$

For K_B

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	1	0
1	X	X	1	0

$K_B = Q_A$

For J_A

Q_C \ Q_BQ_A	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$J_A = 1$

For K_A

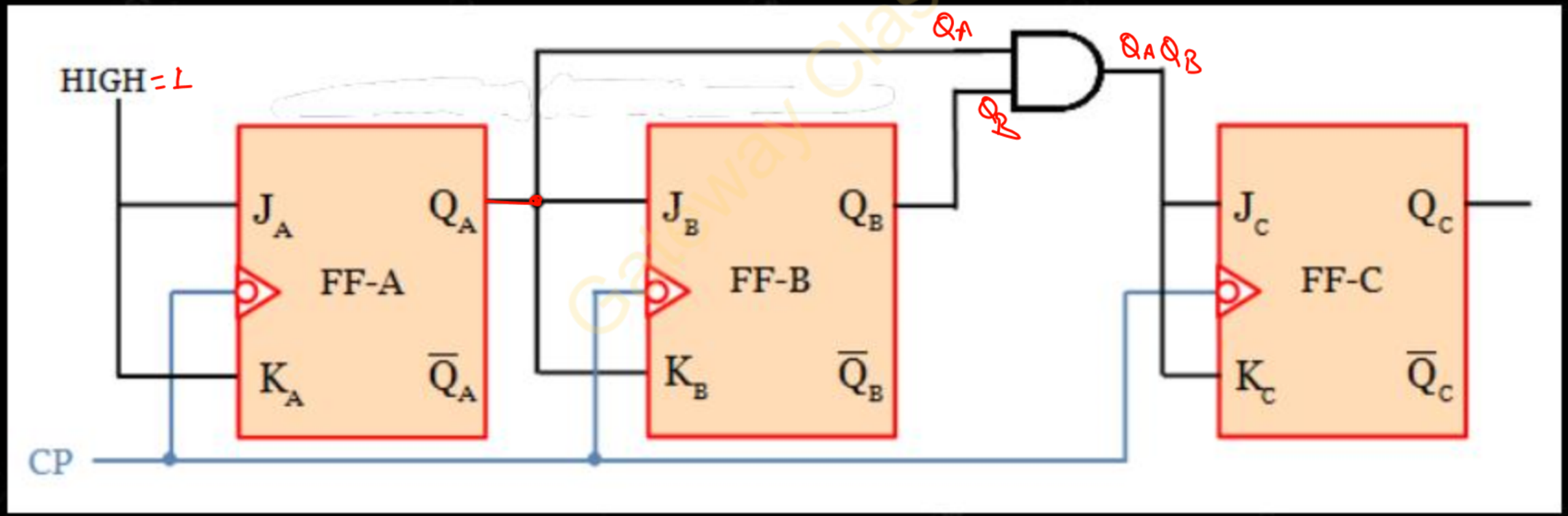
Q_C \ Q_BQ_A	00	01	11	10
0	X	1	1	X
1	X	1	1	X

$K_A = 1$

Gateway Classes

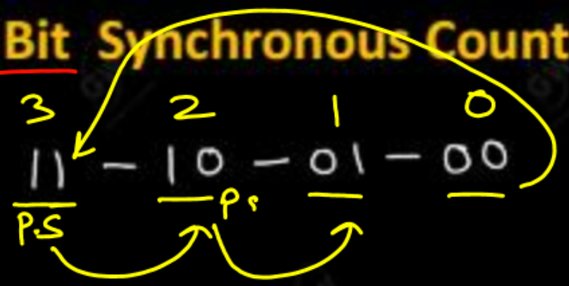
Step 6: Draw the logic diagram of the counter.

The logic diagram of the 3-bit synchronous counter is drawn as follows. Draw the 3 JK flip-flops. The common clock pulse input is given to all the flip-flops. The inputs for each flip-flop are drawn as per the logic functions derived in the previous step. $J_C = K_C = Q_A Q_B$, $J_B = K_B = Q_A$, $J_A = K_A = 1$

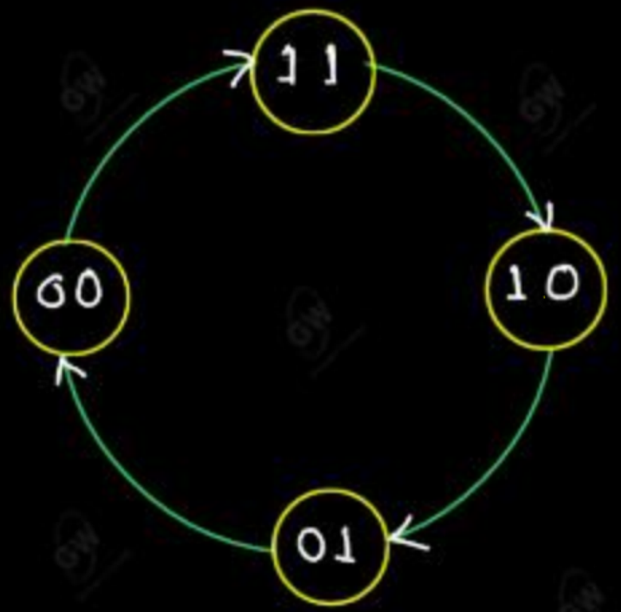


Gateway Classes

2- Bit Synchronous Counter (Down)



CLK	Present I/P		Next I/P		FF I/P				
	Q_B	Q_A	Q_{B+1}	Q_{A+1}	J_B	K_B	J_A	K_A	
1	1	1	1	0	X	0	X	1	3
2	1	0	0	1	X	1	1	X	2
3	0	1	0	0	0	X	X	1	1
4	0	0	1	1	1	X	1	X	0



Excitation Table.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Gateway Classes

2- Bit Synchronous Counter (Down)

Q_B \ Q_A	0	1
0	1 (0)	(1)
1	X (2)	X (3)

$J_B = \bar{Q}_A$ ✓

Q_B \ Q_A	0	1
0	X	X
1	1	

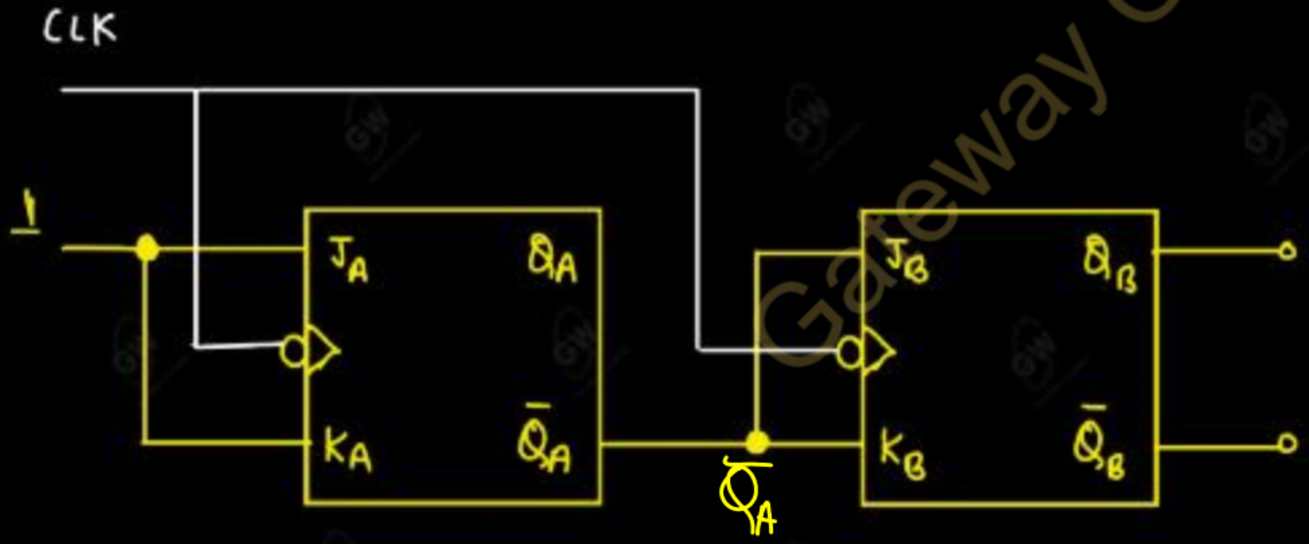
$K_B = \bar{Q}_A$

Q_B \ Q_A	0	1
0	1	X
1	1	X

$J_A = 1$

Q_B \ Q_A	0	1
0	X	1
1	X	1

$K_A = 1$



" 2 Bit Down Counter "

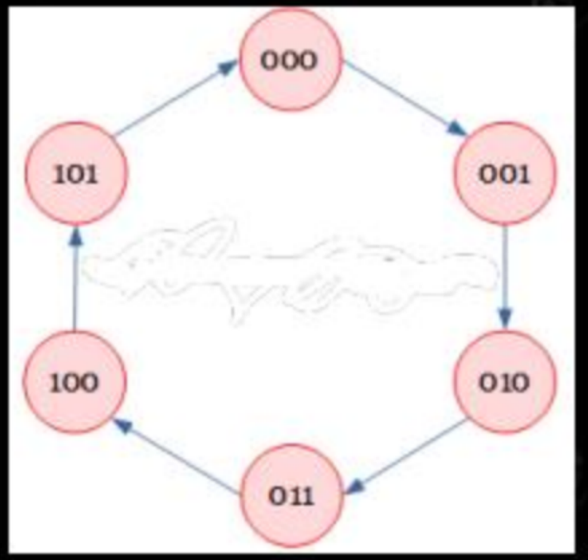
Gateway Classes

Ex. Design a MOD-6 Counter Using JK FF.

000 — 101
0,1,2,3,4,5 → 101

Mod-6 counter represents that the counter will have 6 states (001 to 110). Thus, N = 6. That is the number of flip-flops, n = 3.

The state diagram for the mod-6 counter with 6 states is drawn as below.



The excitation table for JK flip flop is given by,

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Gateway Classes

Excitation table for MOD-6 counter

Clock	Present State			Next State			Flip flop Inputs					
	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
1	0	0	0	0	0	1	0	X	0	X	1	X
2	0	0	1	0	1	0	0	X	1	X	X	1
3	0	1	0	0	1	1	0	X	X	0	1	X
4	0	1	1	1	0	0	1	X	X	1	X	1
5	1	0	0	1	0	1	X	0	0	X	1	X
6	1	0	1	0	0	0	X	1	0	X	X	1
-	1	1	0	X	X	X	X	X	X	X	X	X
-	1	1	1	X	X	X	X	X	X	X	X	X

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Gateway Classes

Derive the flip flop input functions.

For J_C

Q_C \ Q_BQ_A	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_C = Q_BQ_A$

For K_C

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	X	X
1	0	1	X	X

$K_C = Q_A$

For J_B

Q_C \ Q_BQ_A	00	01	11	10
0	0	1	X	X
1	0	0	X	X

$J_B = \overline{Q}_C Q_A$

For K_B

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	1	0
1	X	X	X	X

$K_B = Q_A$

For J_A

Q_C \ Q_BQ_A	00	01	11	10
0	1	X	X	1
1	1	X	X	X

$J_A = 1$

For K_A

Q_C \ Q_BQ_A	00	01	11	10
0	X	1	1	X
1	X	1	X	X

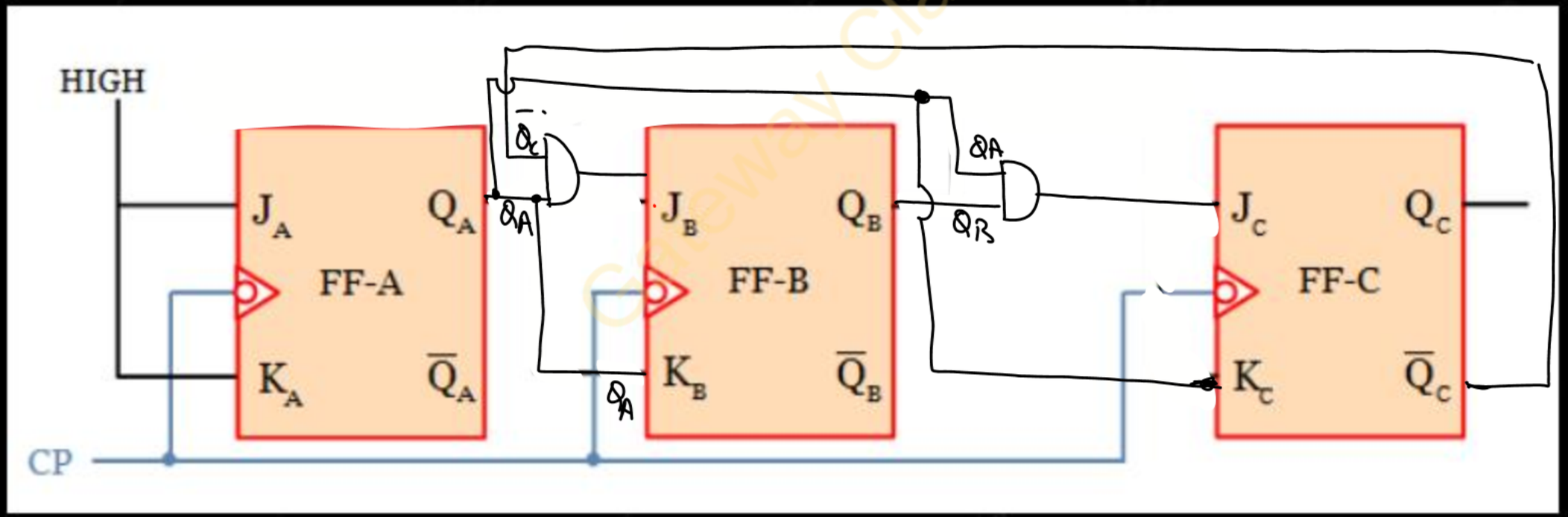
$K_A = 1$

Gateway Classes

Step 6: Draw the logic diagram of the counter.

$J_A = K_A = 1$, $J_B = Q_A \bar{Q}_C$, $K_B = Q_A$, $J_C = Q_A Q_B$, $K_C = Q_A$

MOD- 6 Counter



Gateway Classes

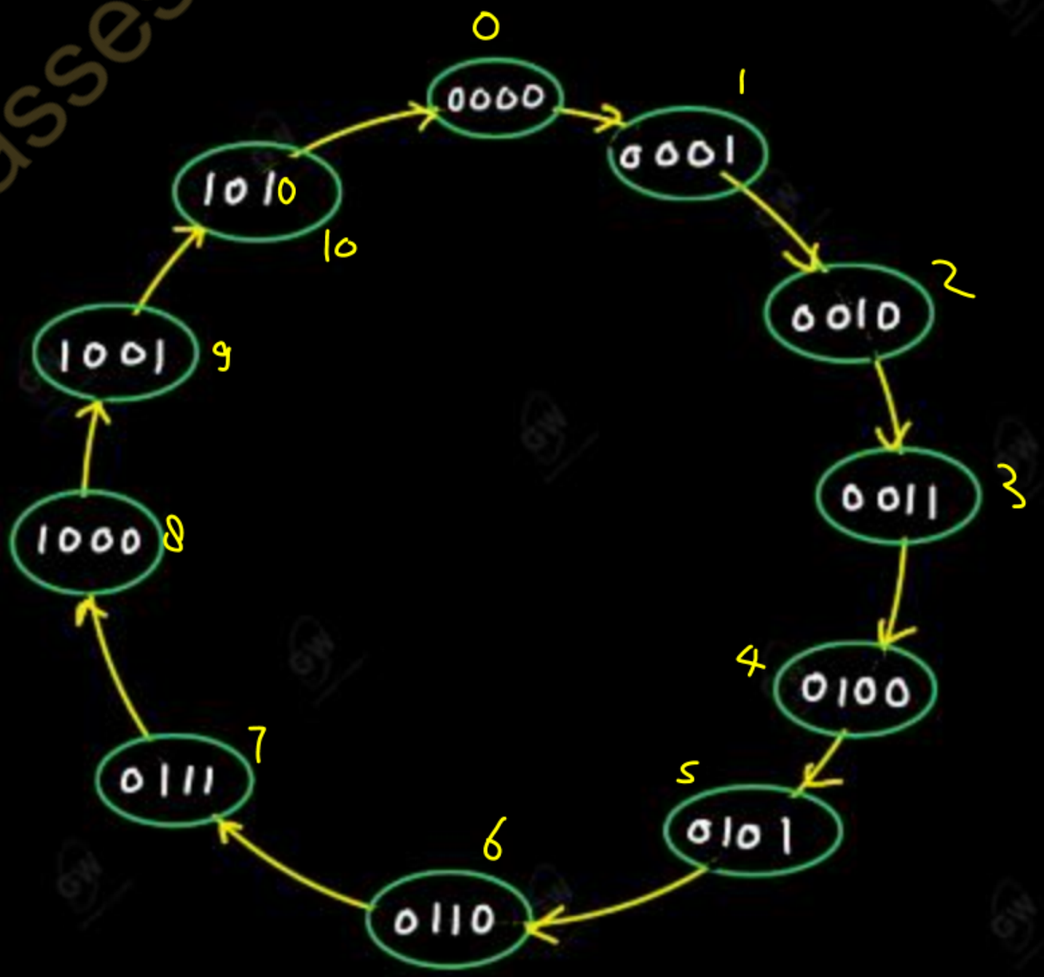
Ex. Design a MOD-11 Counter Using T FF.

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Mod-6 counter represents that the counter will have 11 states (0001 to 1010). Thus, N = 11. That is the number of flip-flops, n = 4.

The state diagram for the mod-6 counter with 11 states is drawn as below.

The excitation table for T flip flop is given by,



Gateway Classes

Excitation table for MOD-11 counter

	Present state				Next state				Inputs.				
CLK	Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_D	T_C	T_B	T_A	
1	0	0	0	0	0	0	0	1	0	0	0	1	0
2	0	0	0	1	0	0	1	0	0	0	1	1	1
3	0	0	1	0	0	0	1	1	0	0	0	1	2
4	0	0	1	1	0	1	0	0	0	1	1	1	3
5	0	1	0	0	0	1	0	1	0	0	0	1	4
6	0	1	0	1	0	1	1	0	0	0	1	1	5
7	0	1	1	0	0	1	1	1	0	0	0	1	6
8	0	1	1	1	1	0	0	0	1	1	1	1	7
9	1	0	0	0	1	0	0	1	0	0	0	1	8
10	1	0	0	1	1	0	1	0	0	0	1	1	9
11	1	0	1	0	0	0	0	0	1	0	1	0	10
12	1	0	1	1	x	x	x	x	x	x	x	x	11
13	1	1	0	0	x	x	x	x	x	x	x	x	12
14	1	1	0	1	x	x	x	x	x	x	x	x	13
15	1	1	1	0	x	x	x	x	x	x	x	x	14
16	1	1	1	1	x	x	x	x	x	x	x	x	15

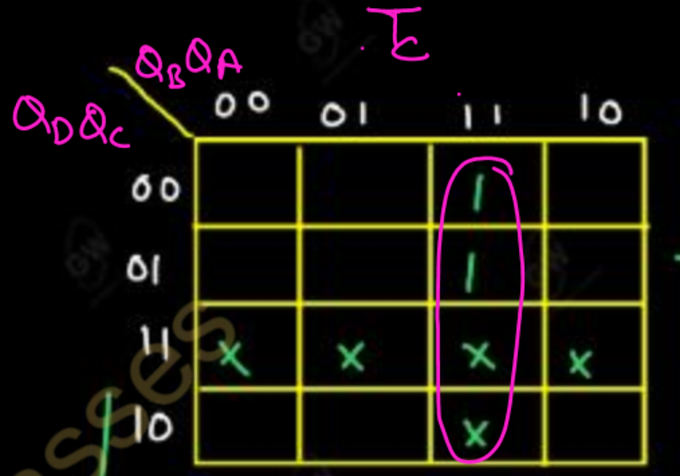
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Gateway Classes

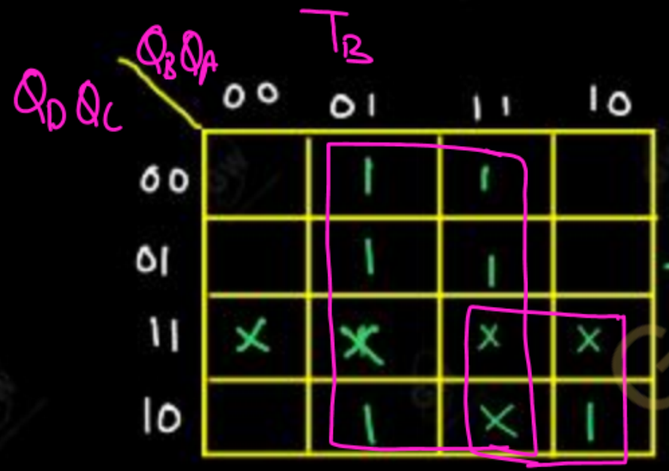
Derive the flip flop input functions.



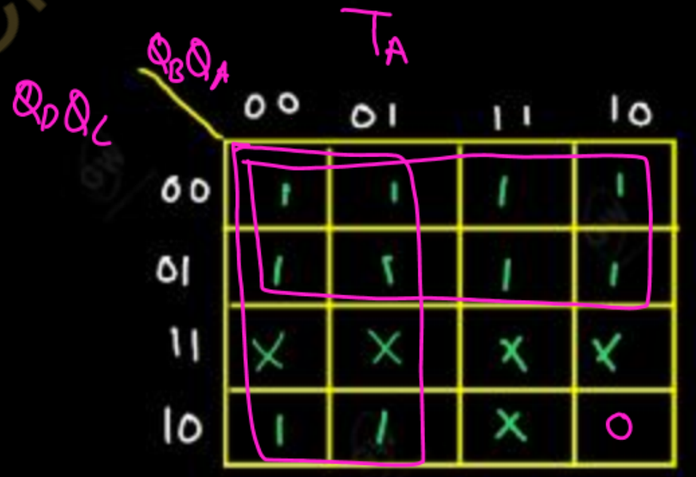
$T_D = Q_B Q_D + Q_B Q_A Q_C$



$T_C = Q_B Q_A$



$T_B = Q_A + Q_B Q_D$



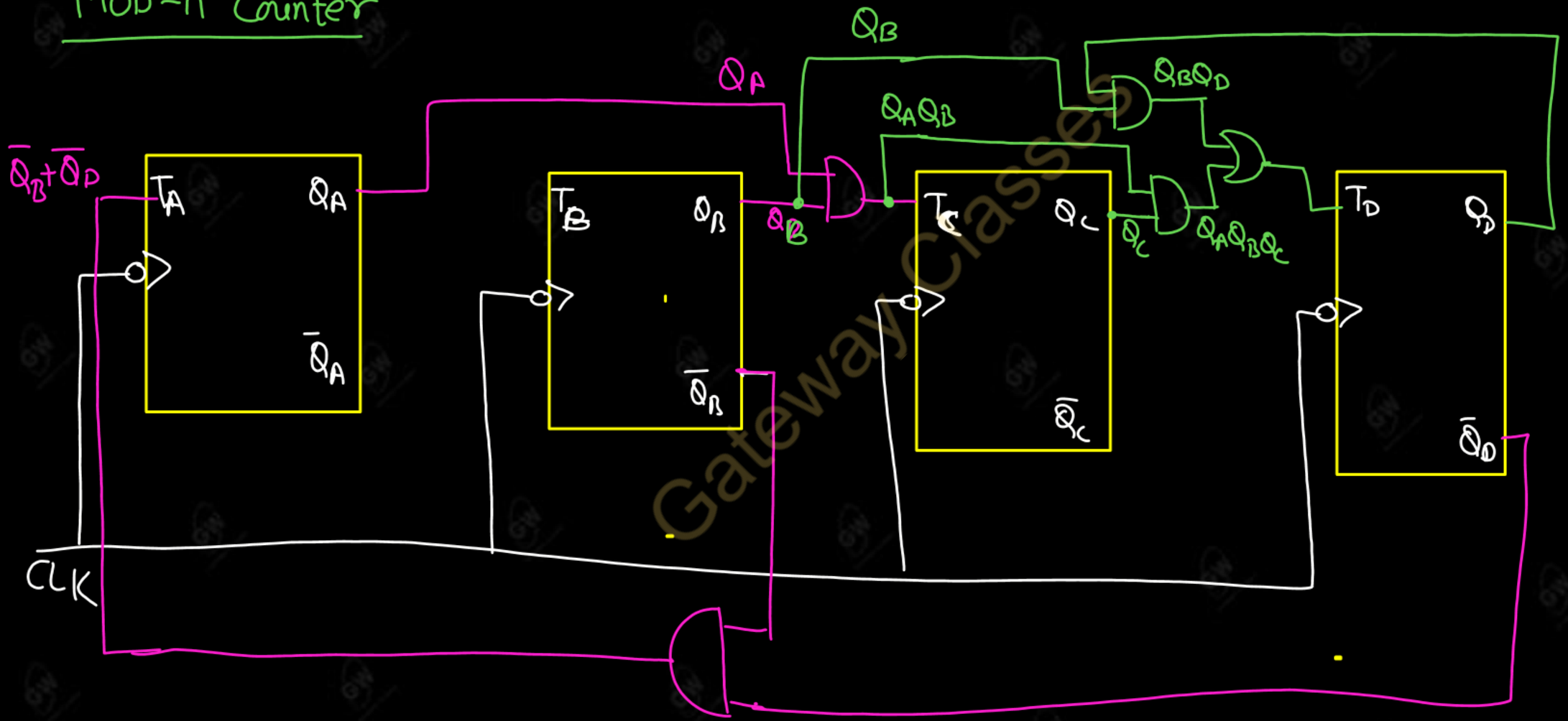
$T_A = \overline{Q_D} + \overline{Q_B}$

Gateway Classes

Logic diagram of the counter.

$T_D = Q_B Q_D + Q_A Q_B Q_C$, $T_C = Q_A Q_B$, $T_B = Q_A + Q_B Q_D$, $T_A = \overline{Q}_B + \overline{Q}_D$

MOD-11 Counter

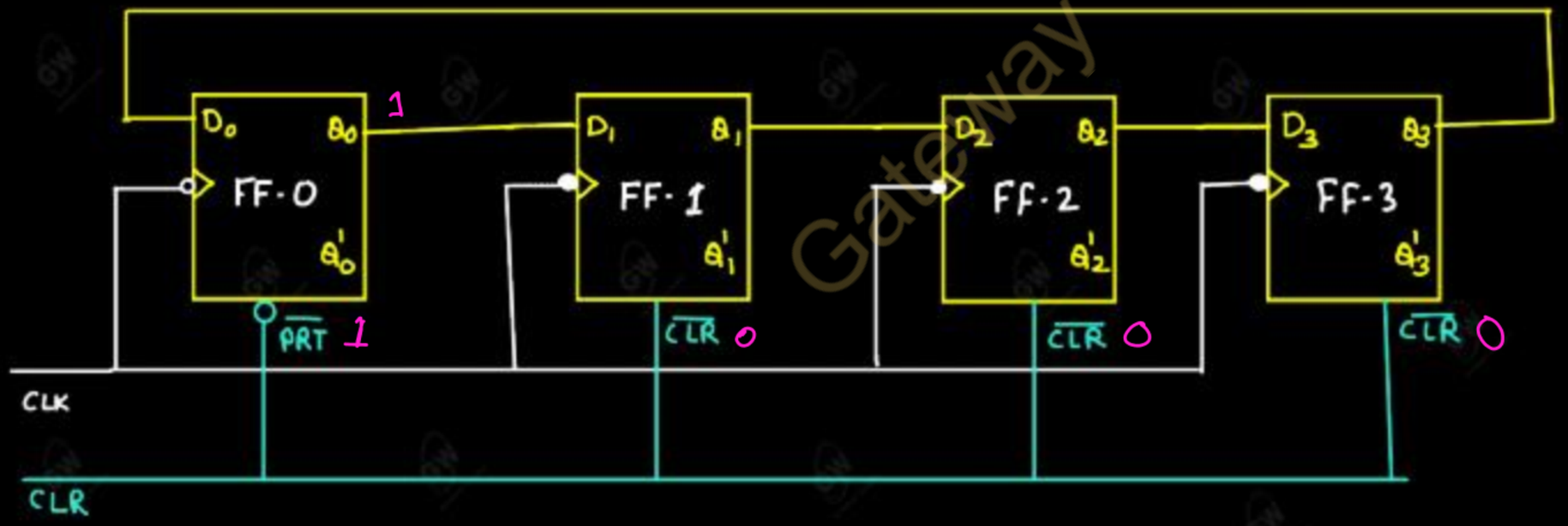


Gateway Classes

Ring counter:

The ring counter is a application of shift register, in which the output of last flip flop is connected to input of first flip flop. In ring counter if the output of any flip flop is 1, then the output of remaining flip flops is 0. The Ring counters transfers the same output throughout the circuit. in a four-register counter, with initial register values of 0000, the repeating pattern is 1000 → 0100 → 0010 → 0001 → 1000.

No. of State = 4 , MOD-4



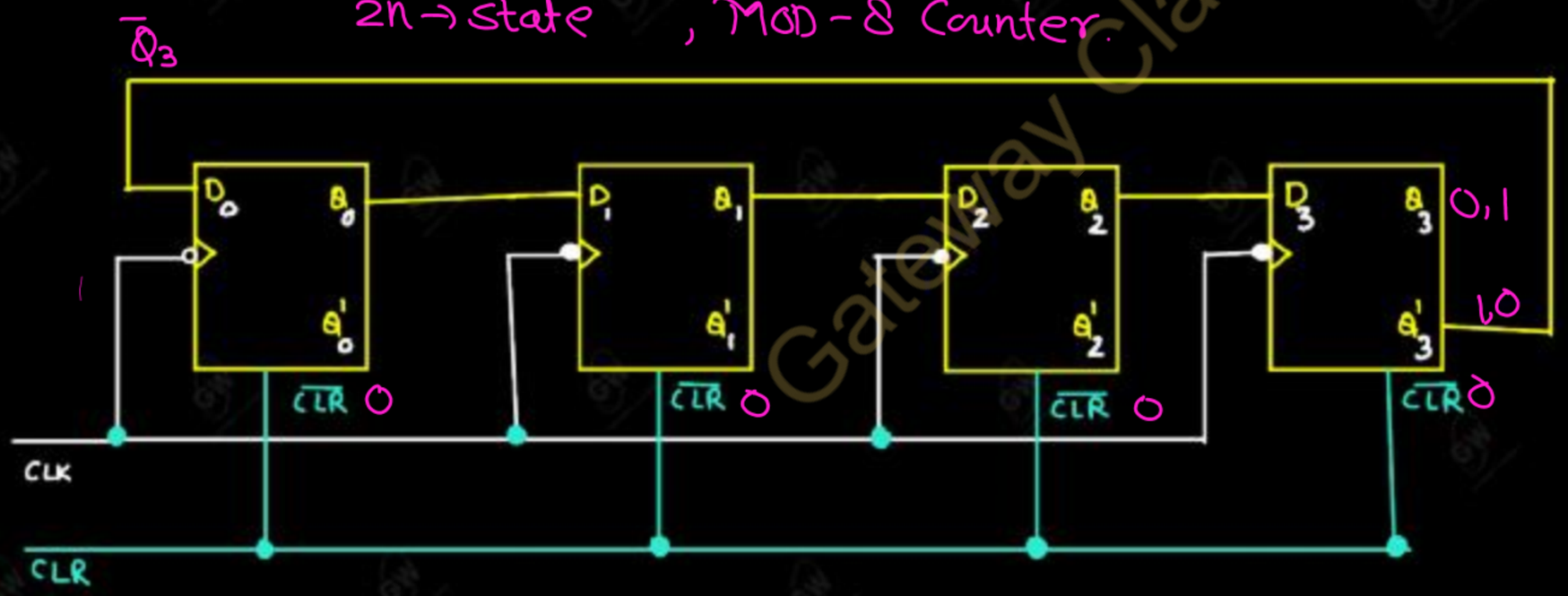
CLK	Q_3	Q_2	Q_1	Q_0	
1	0	0	0	1	1
2	0	0	1	0	2
3	0	1	0	0	4
4	1	0	0	0	8
	0	0	0	1	

Gateway Classes

Johnson's counter or twisted ring counter:

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The Johnson counter is a modification of ring counter. In this the inverted output of the last stage flip flop is connected to the input of first flip flop. If we use n flip flops to design the Johnson counter, it is known as 2n bit Johnson counter or Mod 2n Johnson counter. The Johnson counter circulates a stream of ones followed by zeroes around the ring. For example, in a four-register counter, with initial register values of 0000, the repeating pattern is: 0000, 1000. 1100, 1110, 1111, 0111, 0011, 0001, 0000...

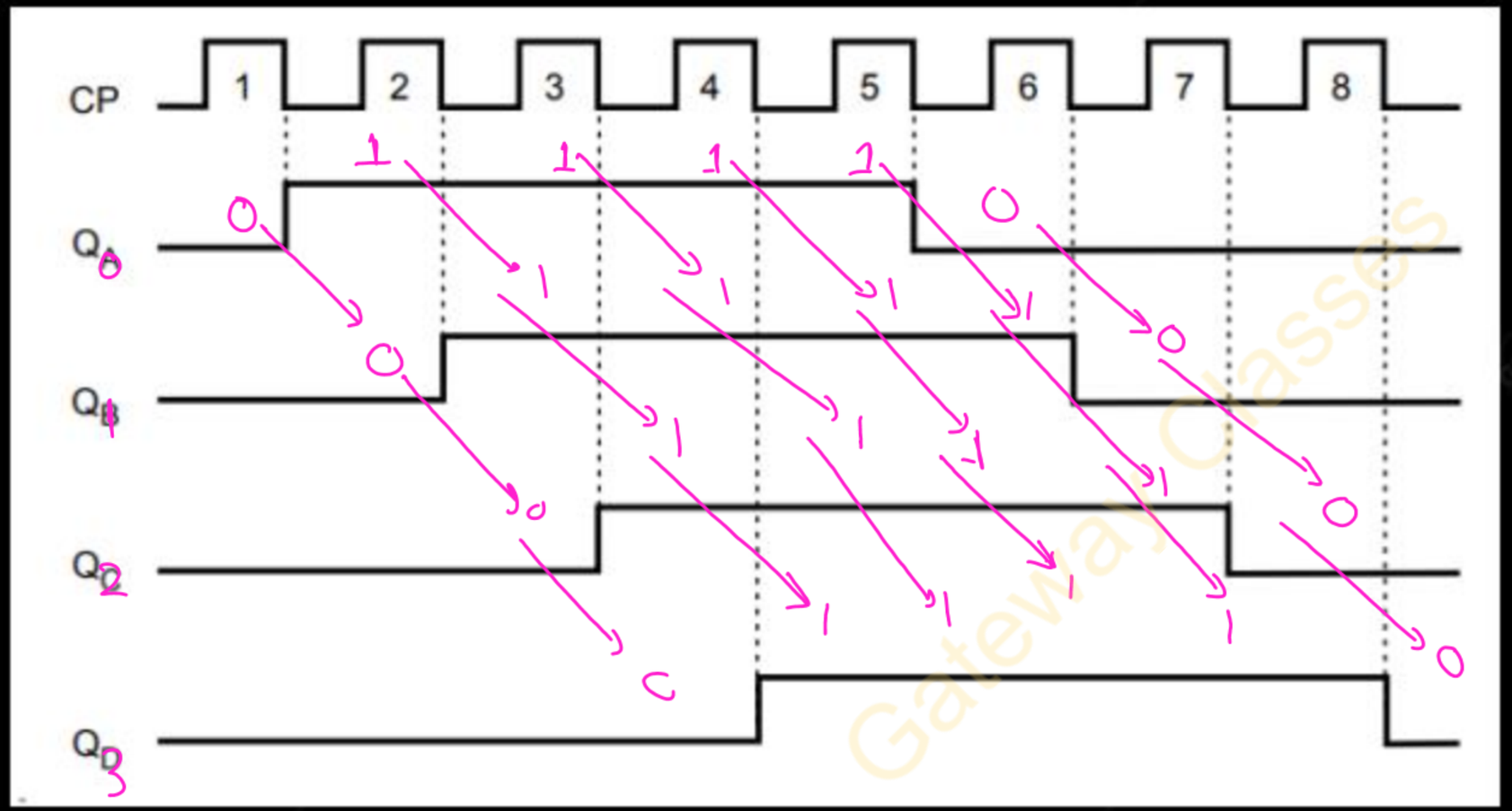


CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1
5	1	1	1	0
6	1	1	0	0
7	1	0	0	0

Gateway Classes

Johnson's counter or twisted ring counter:

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Mod - 2n Counter

No. of flip flop = n

No. of state = 2n

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Thank You

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